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TITLE:	DENVERTON_COM_E REFLESH
DESCRIPTION:	DENVERTON_COM_E REFLESH

DESIGNER:	VIVIAN ZHANG
REVIEWER:	MARCO QIN
APPROVER:	TERRY MO

COVER SHEET

Title: DENVERTON_COM_E REFLESH	Designer: Vivian Zhang
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A3 (297X420)

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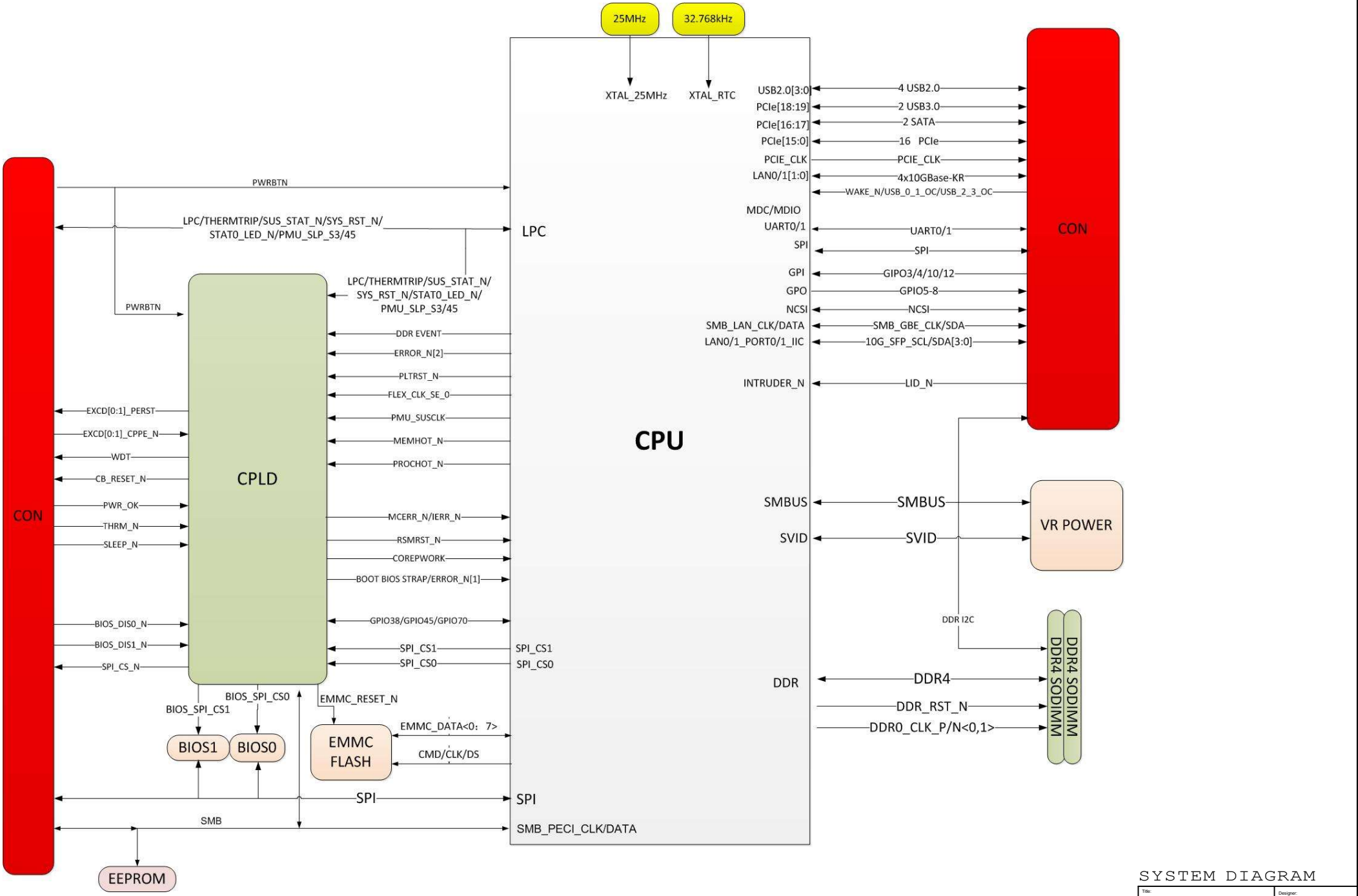
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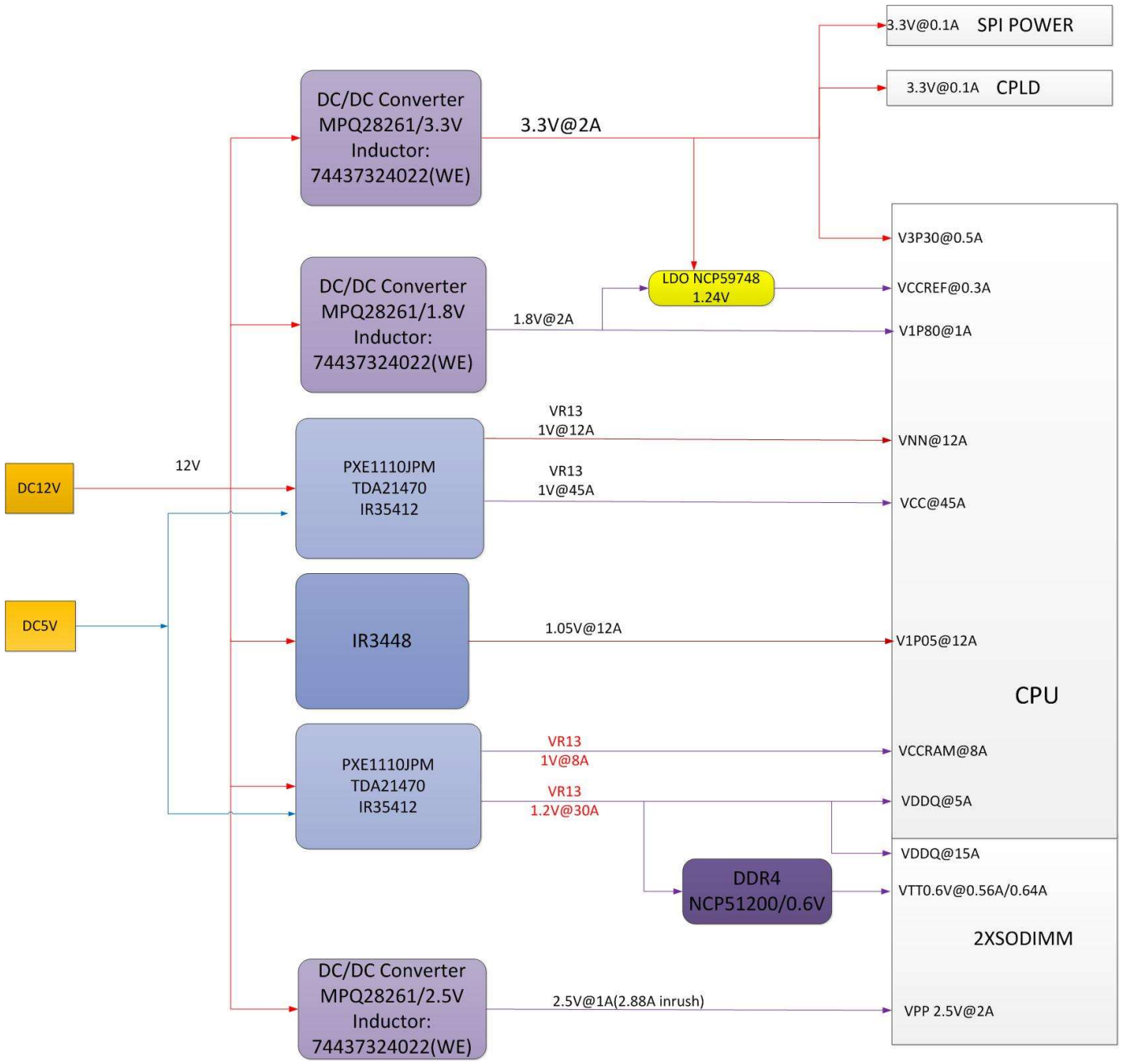
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SYSTEM DIAGRAM

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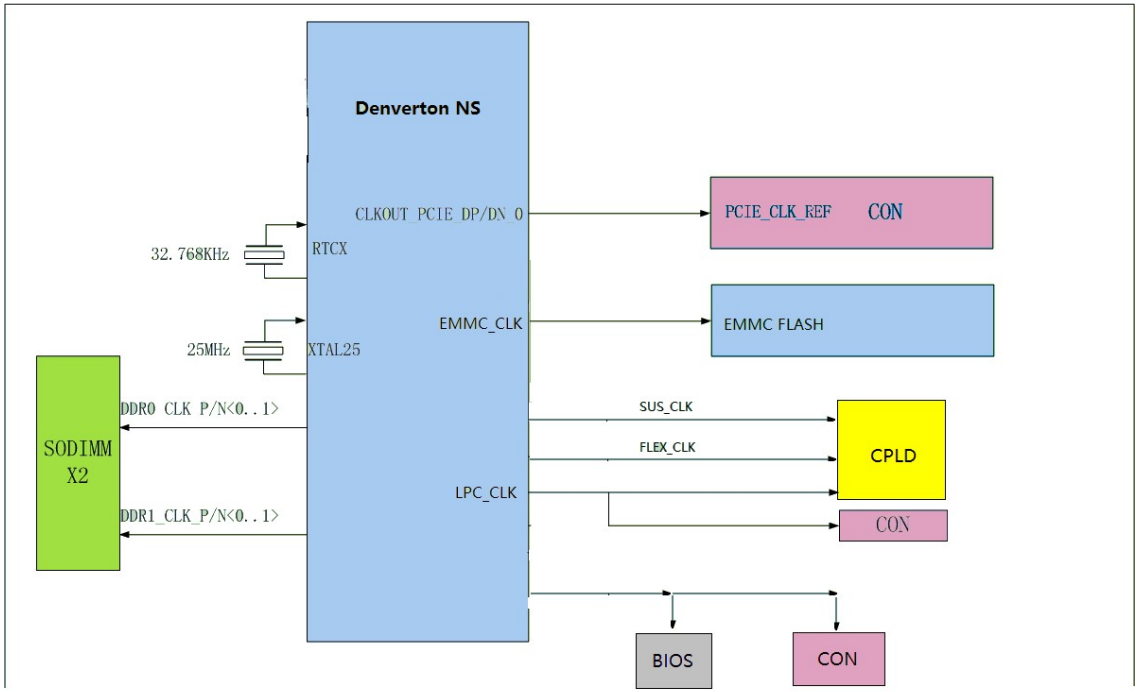
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POWER TOPOLOGY

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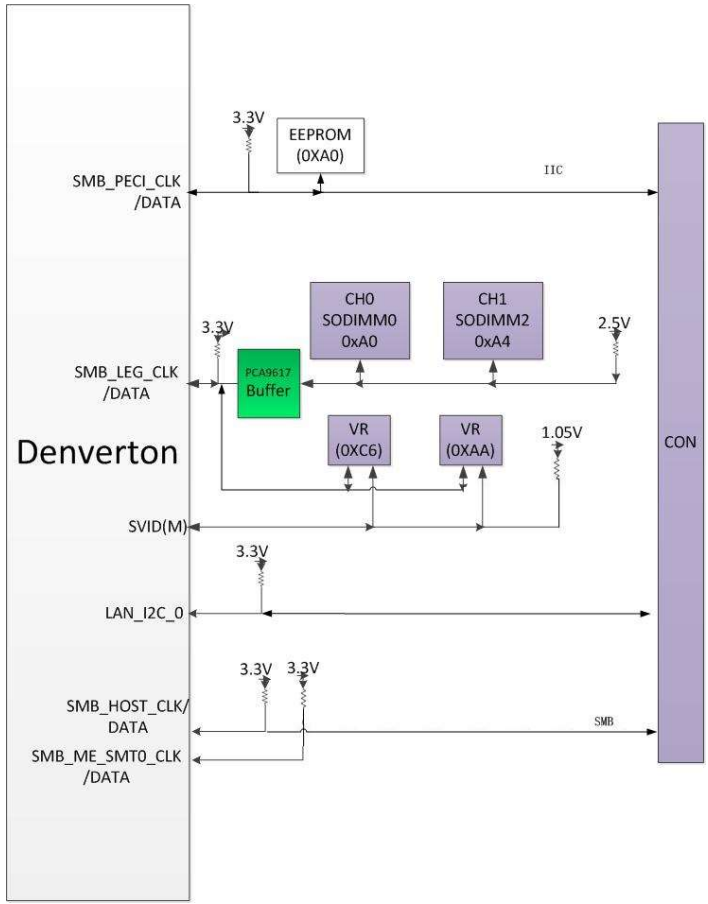
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CLK TOPOLOGY

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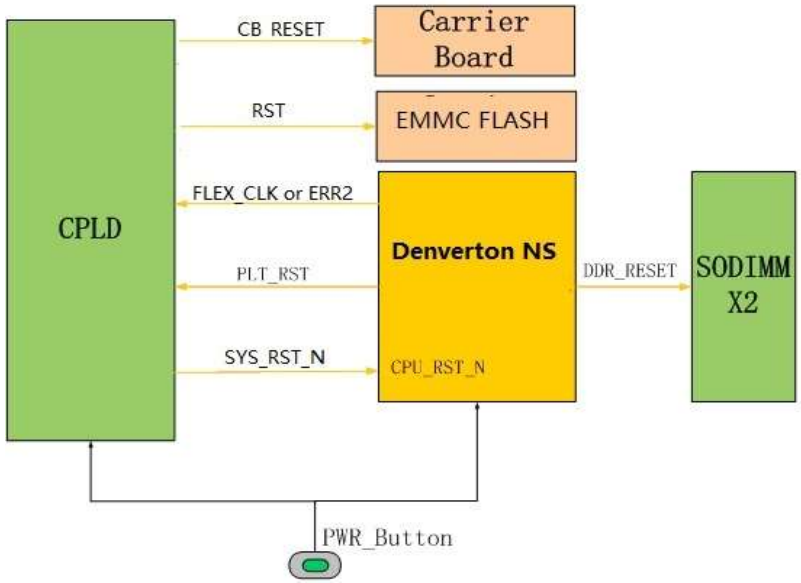
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IIC TOPOLOGY

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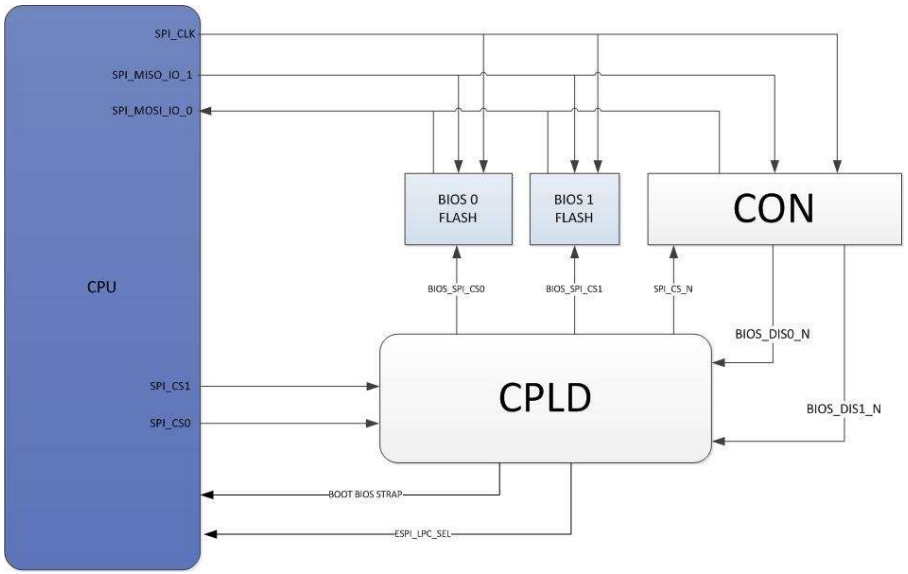
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RST TOPOLOGY

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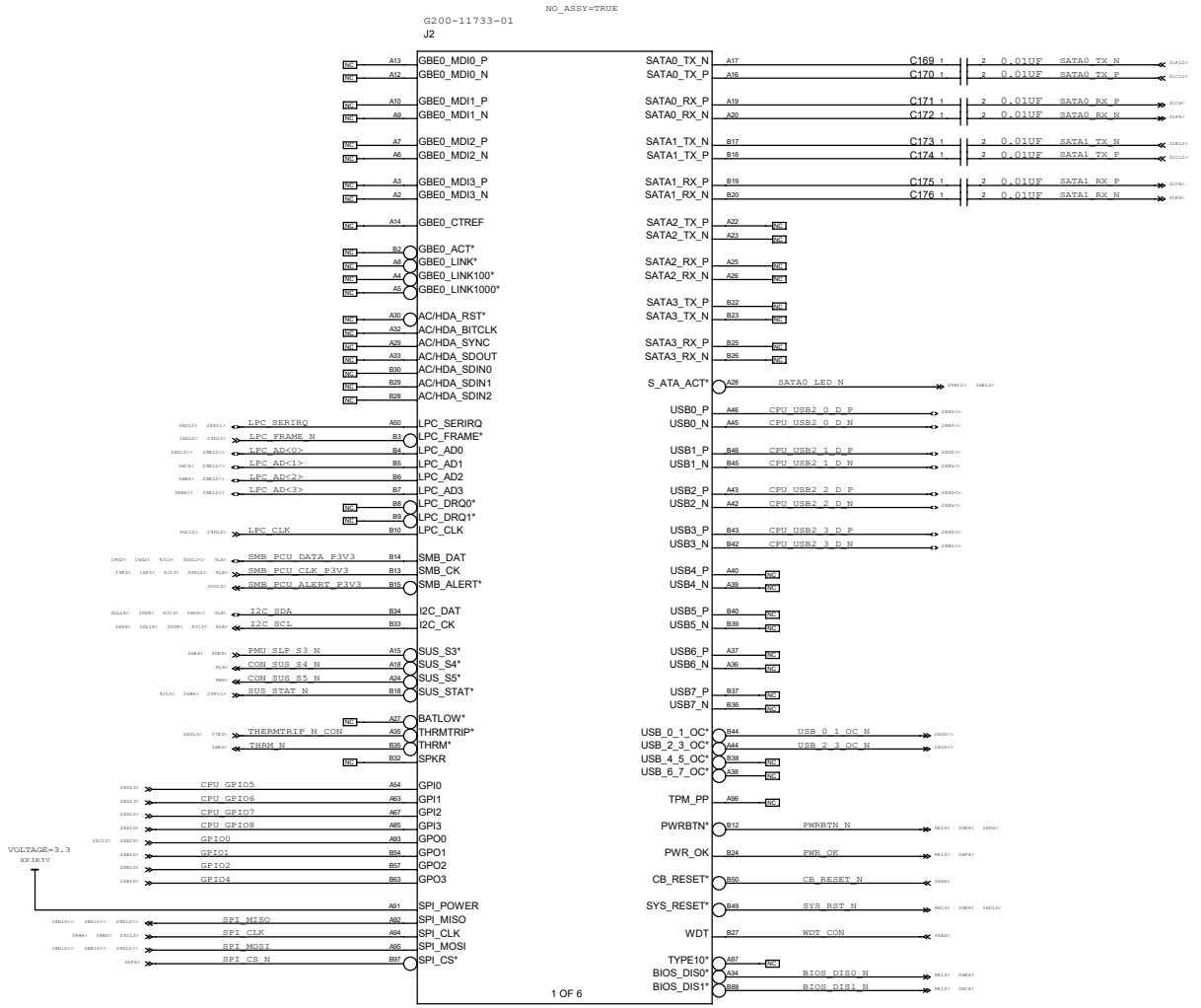
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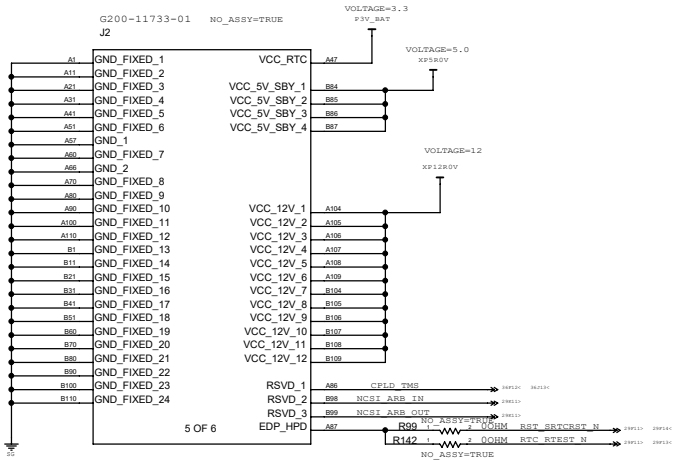


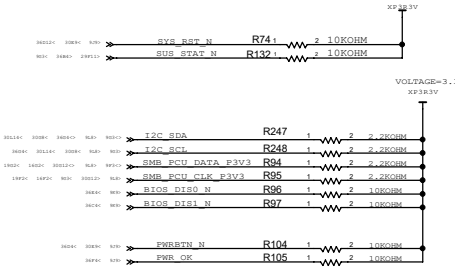
BIOS_DIS0_N	BIOS_DIS1_N	BIOS_SPI_CS0	BIOS_SPI_CS1	SPI_CS_N	BOOT_BIOS_STRAP	ESPI_LPC_SEL
FROM Board	FROM Board	OUT	OUT	OUT	OUT	OUT
0	0	CS0	H	CS1	0	LPC
0	1	CS0	CS1	High	1	LPC
1	0	High	CS1	CS0	0	LPC
1	1	CS0	CS1	High	0	LPC

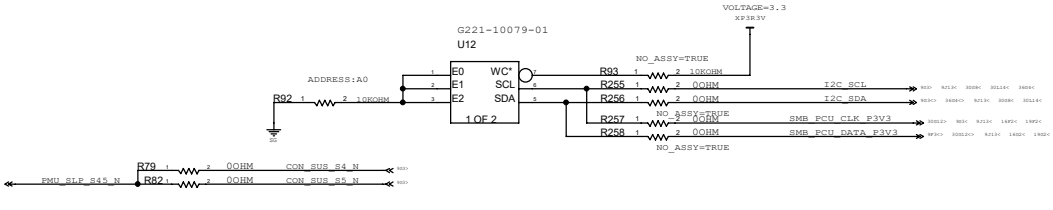
BIOS TOPOLOGY

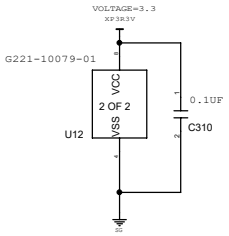
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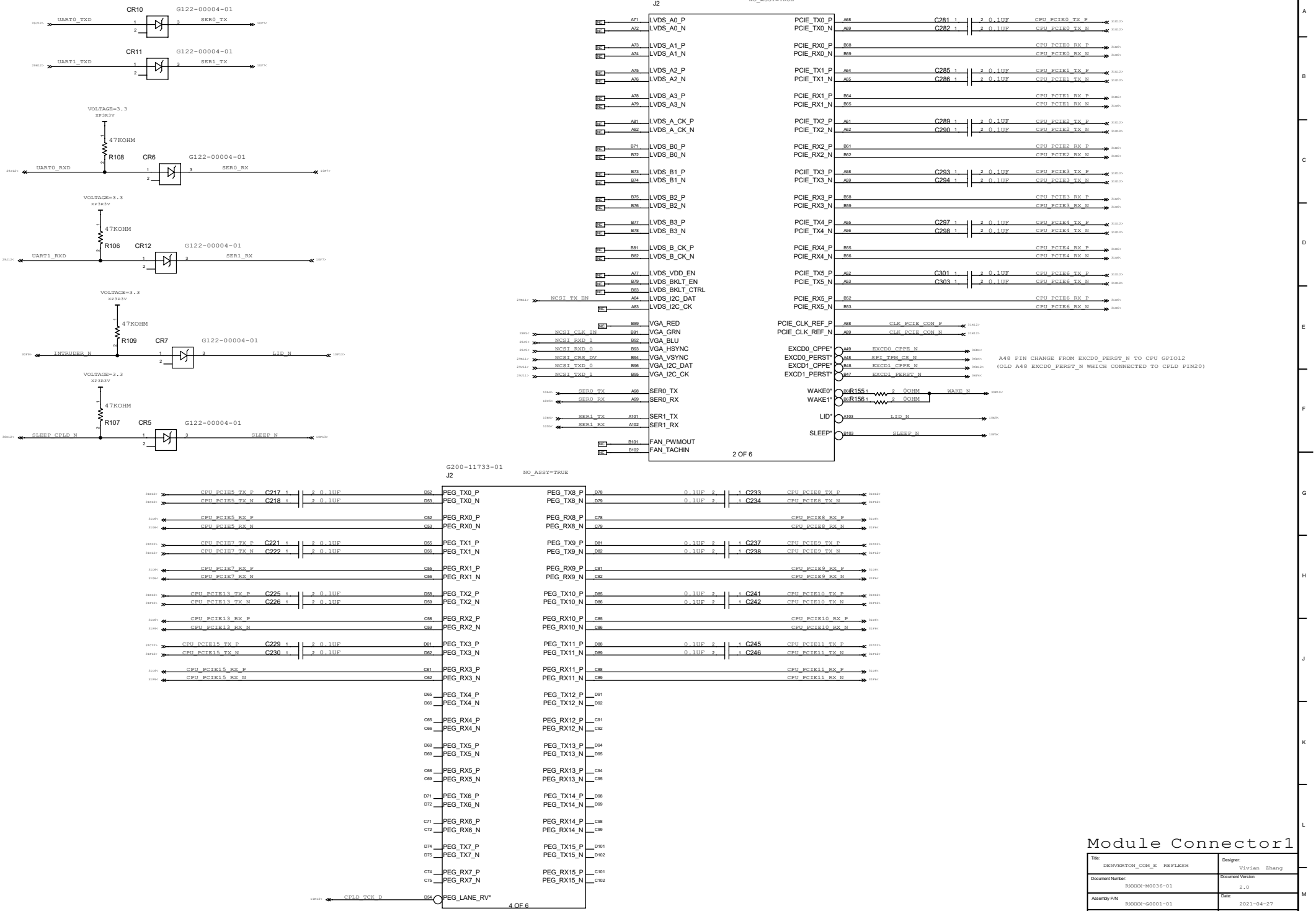




Module Connector0

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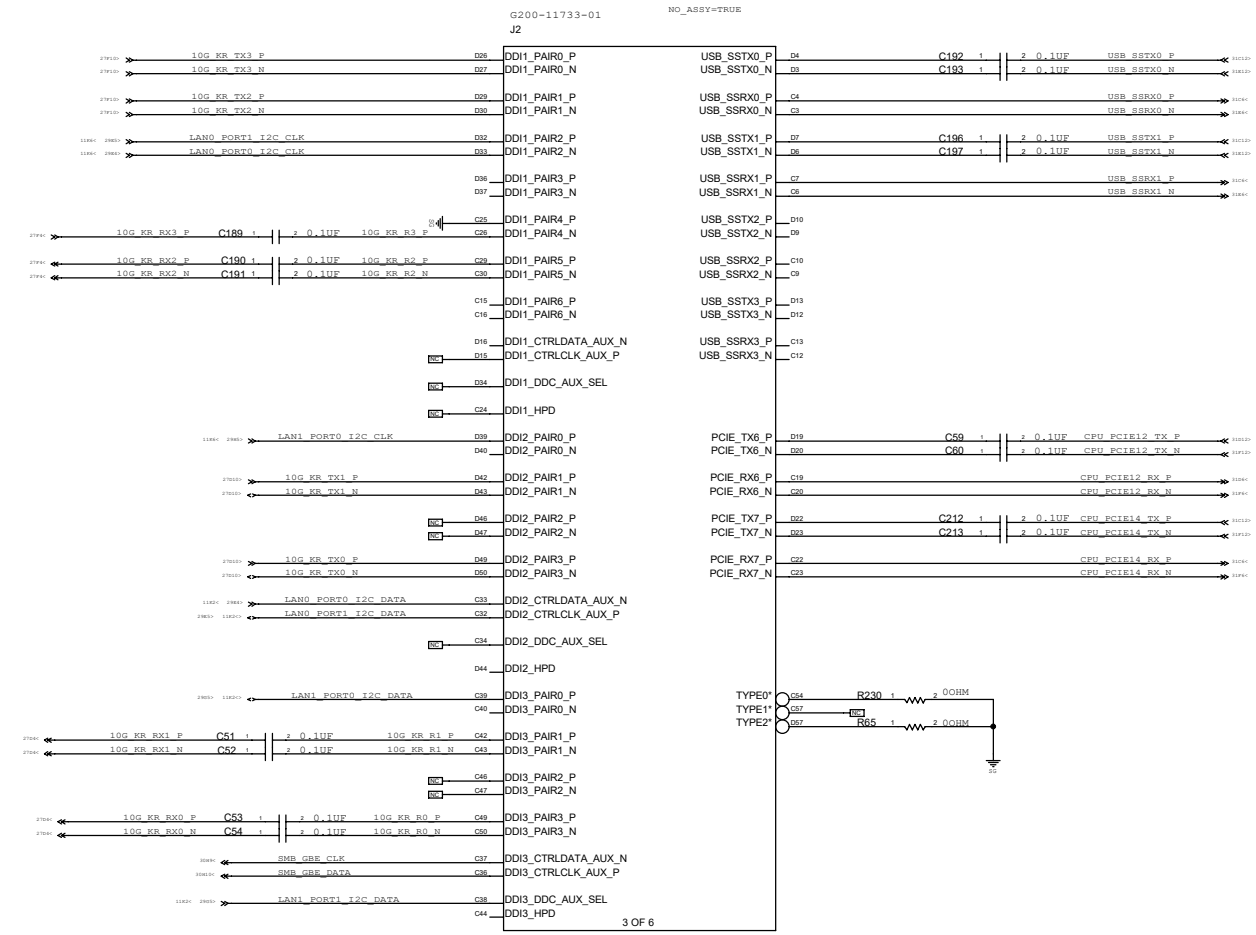
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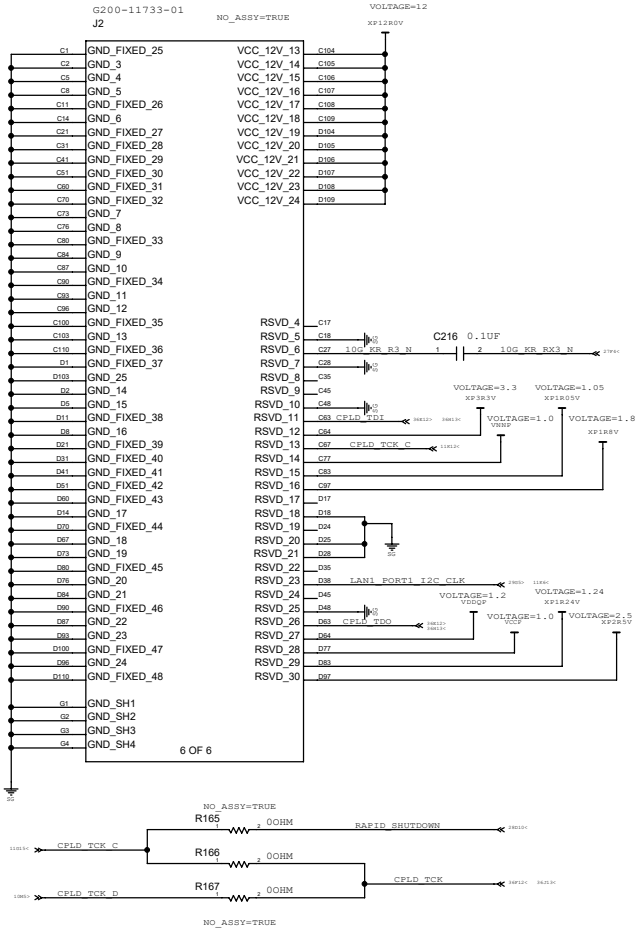


Module Connector1

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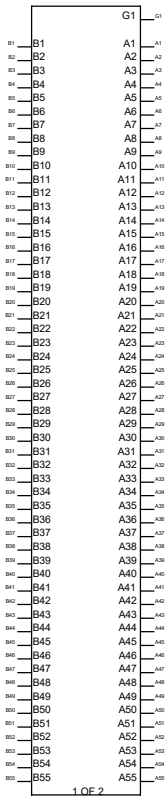


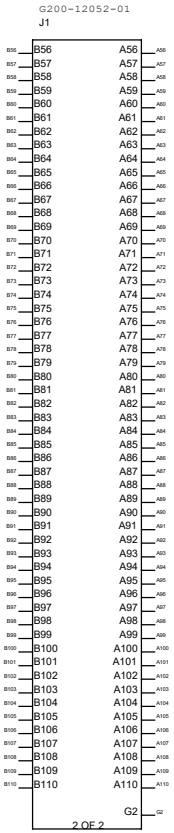


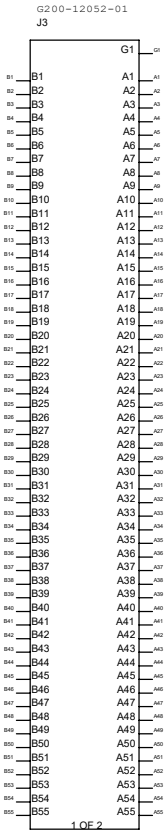
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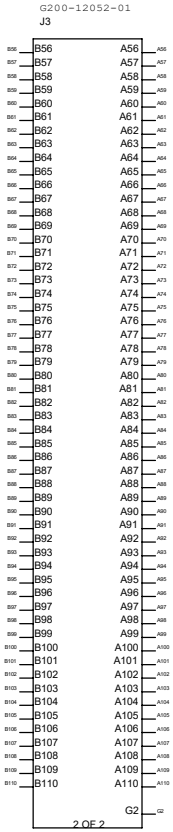
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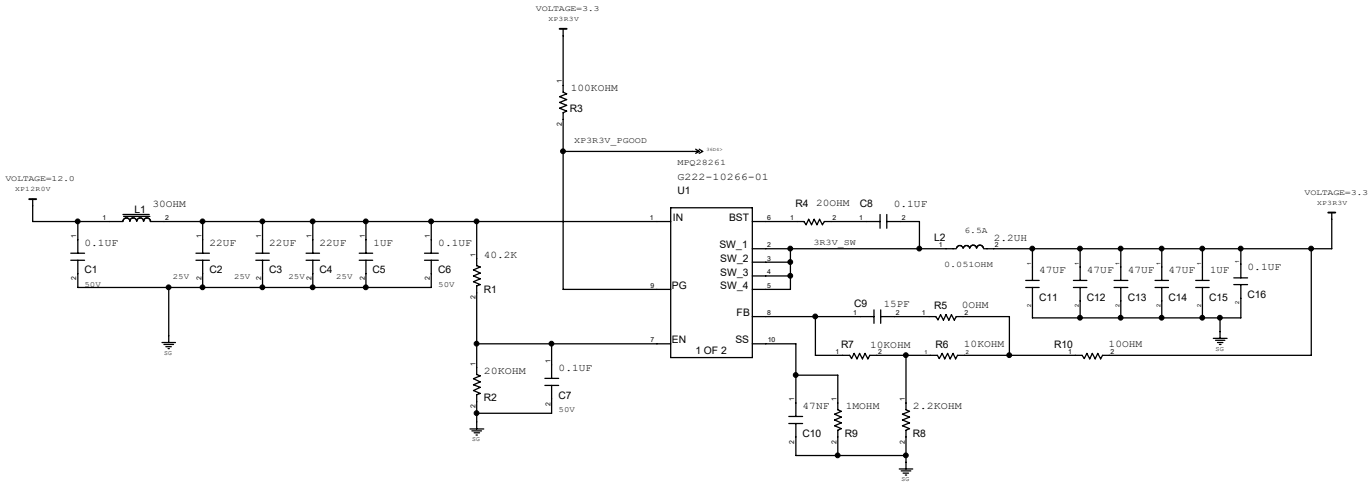


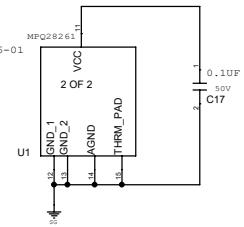


<NEW CONNECTORS>.

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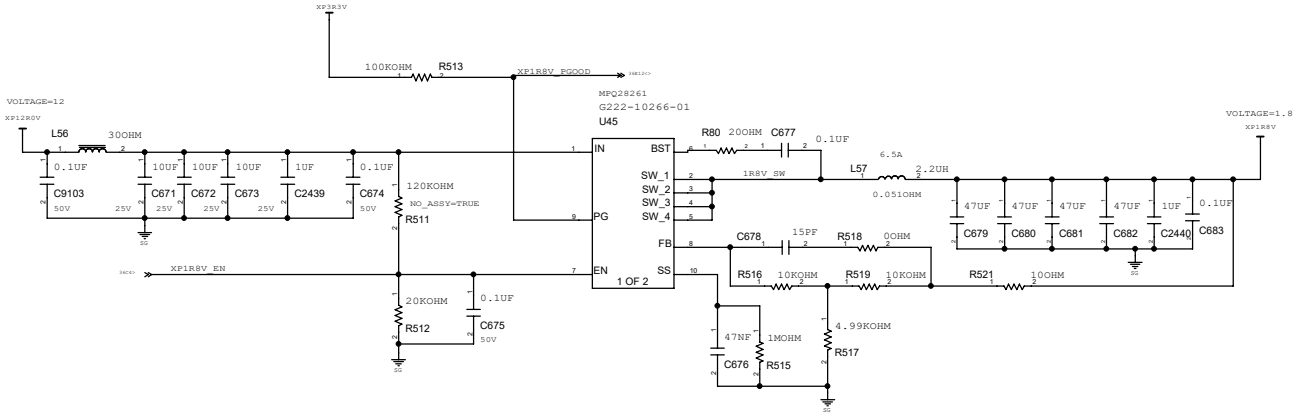


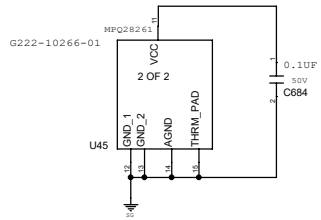


XP3R3V

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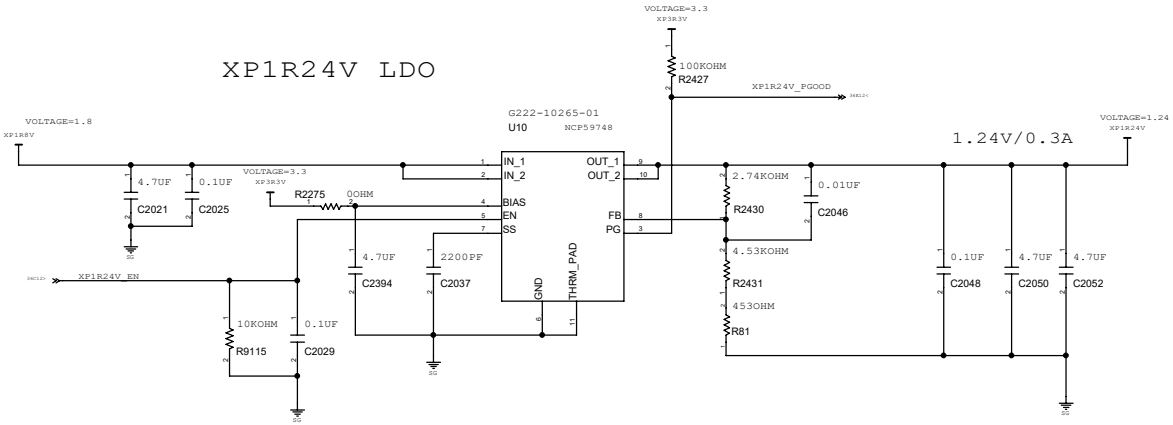
Vo	R517	R516	C678
5.5V	1.21K	10K	NC
5V	1.37K	10K	NC
3.3V	2.2K	12K	15pF
2.5V	3.16K	12K	15pF
1.8V	4.99K	12K	15pF
1.2V	10K	18K	18pF
1.0V	15K	18K	18pF
0.9V	20K	18K	18pF
0.7V	60.4K	18K	33pF

XP1R8V

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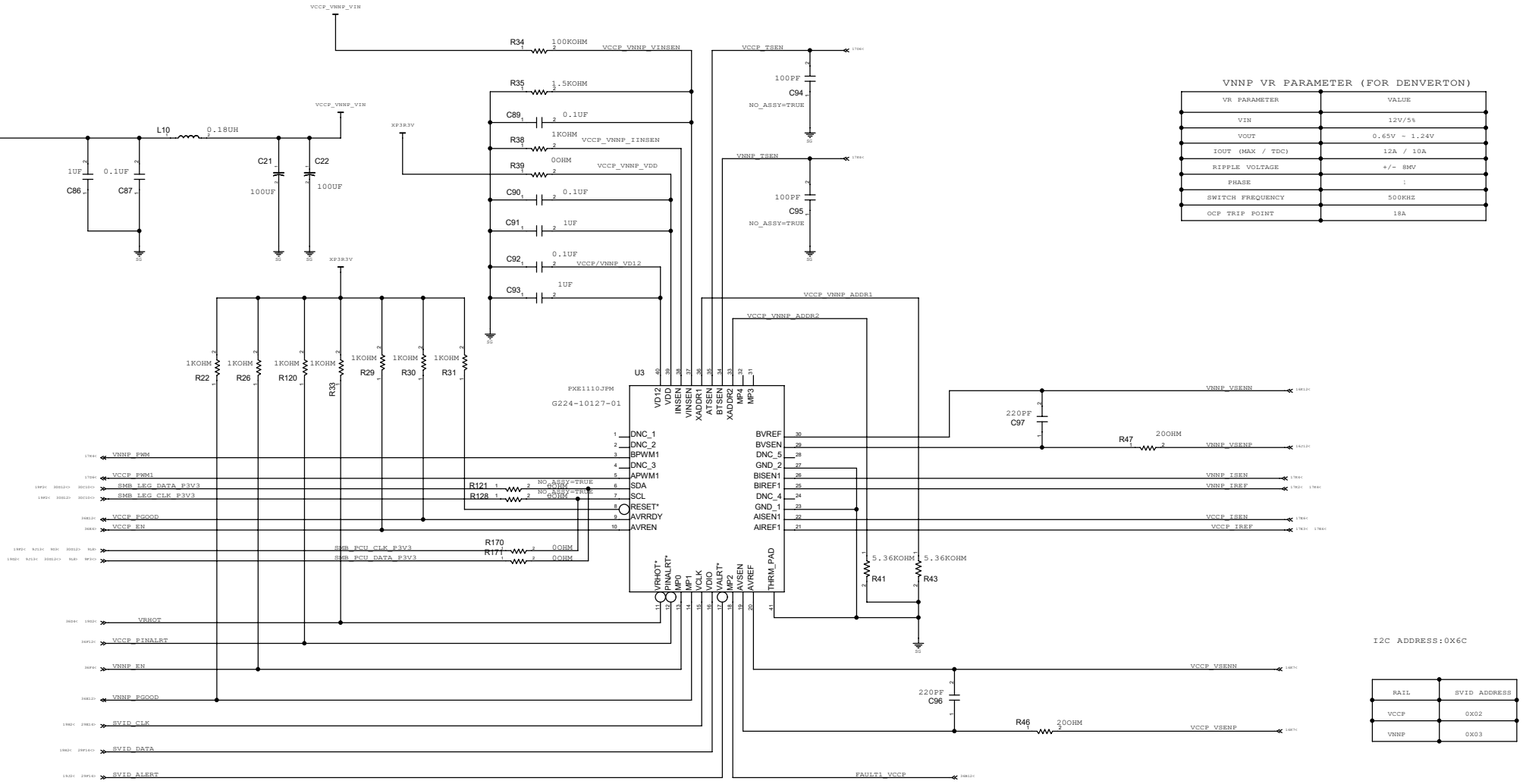
XP1R24V LDO



XP1R24V

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VNNP VR PARAMETER (FOR DENVERTON)

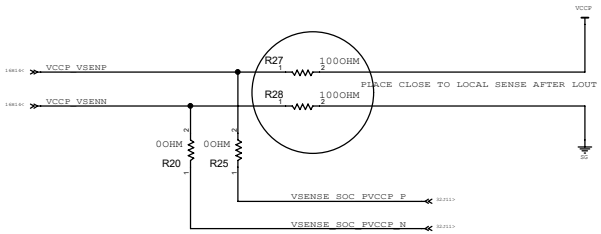
VR PARAMETER	VALUE
VIN	12V/5%
VOUT	0.65V ~ 1.24V
IOUT (MAX / TDC)	12A / 10A
RIPPLE VOLTAGE	+/- 8MV
PHASE	1
SWITCH FREQUENCY	500KHZ
OCP TRIP POINT	18A

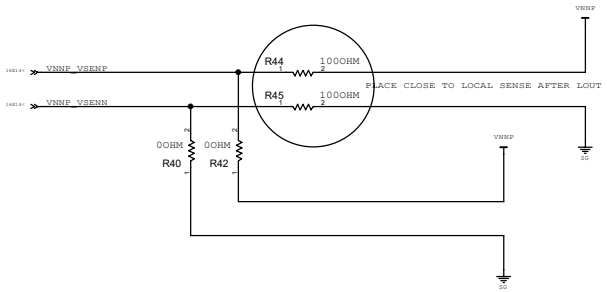
I2C ADDRESS:0X6C

RAIL	SVID ADDRESS
VCCP	0X02
VNNP	0X03

VCCP VR PARAMETER (FOR DENVERTON)

VR PARAMETER	VALUE
VIN	12V/5%
VOUT	0.52V ~ 1.24V
IOUT (MAX / TDC)	45A / 18A
RIPPLE VOLTAGE	+/- 4MV
PHASE	1
SWITCH FREQUENCY	500KHZ
LOADLINE	0.0023OHM
OCP TRIP POINT	60A

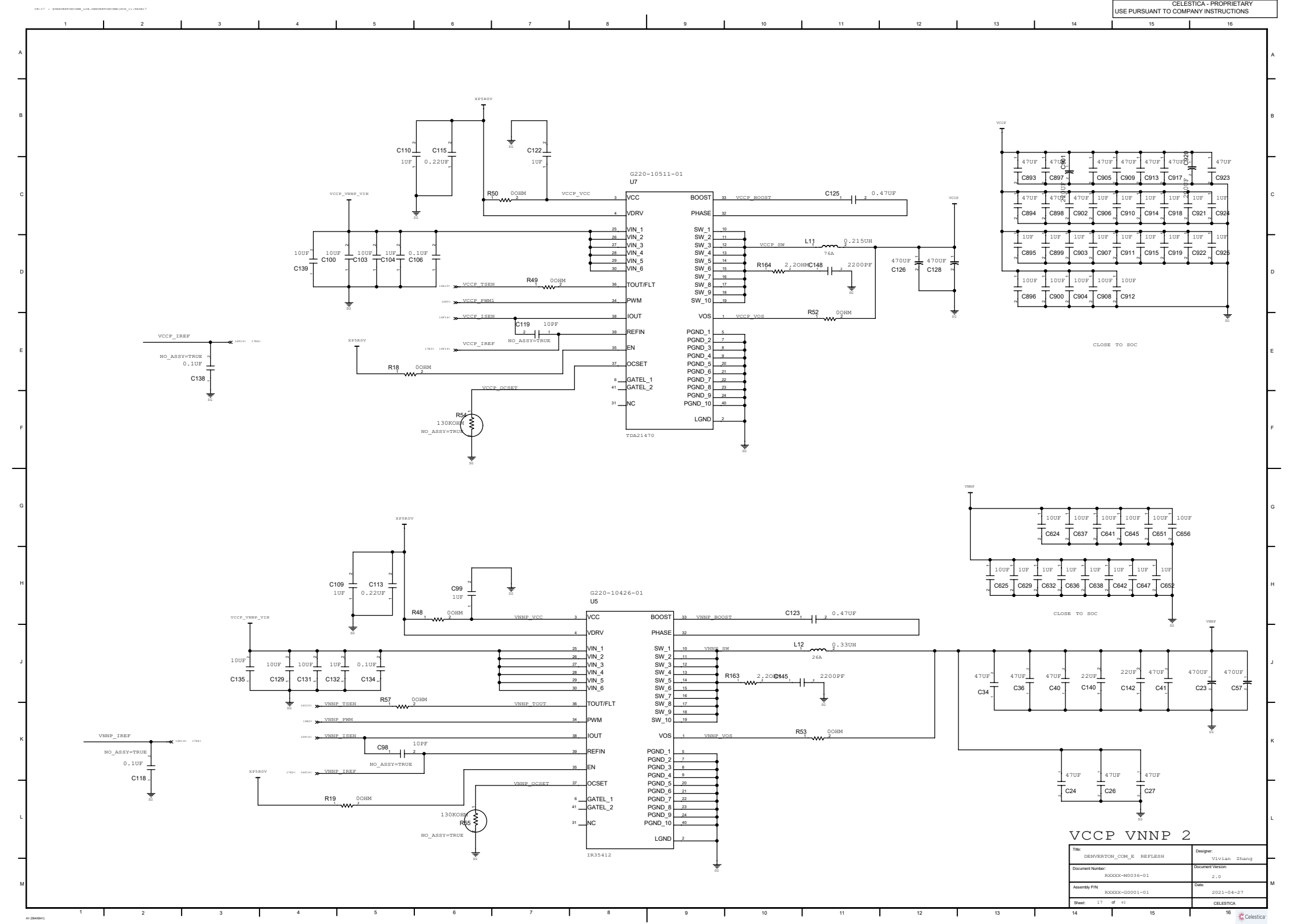




VCCP VNNP 1

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VCCP VNNP 2

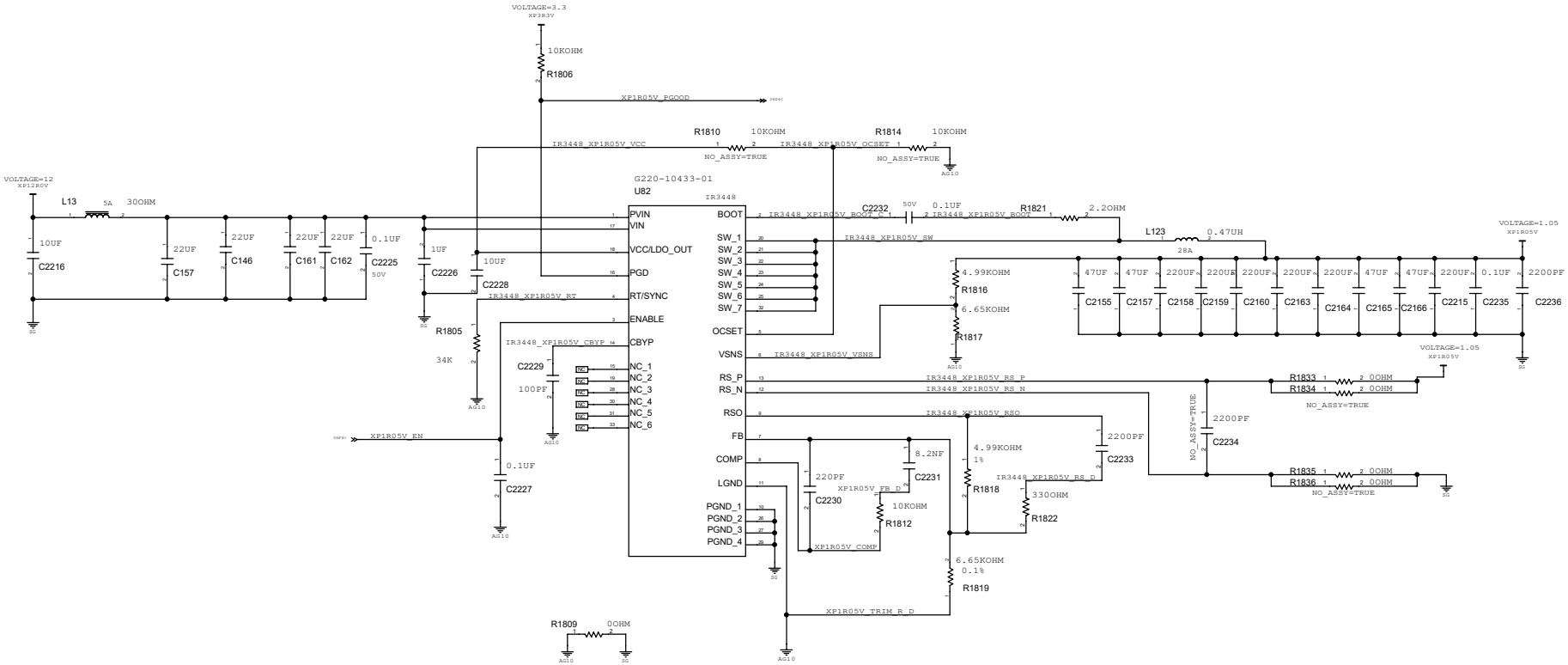
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XP1R05V/12.2A

XP1R05V

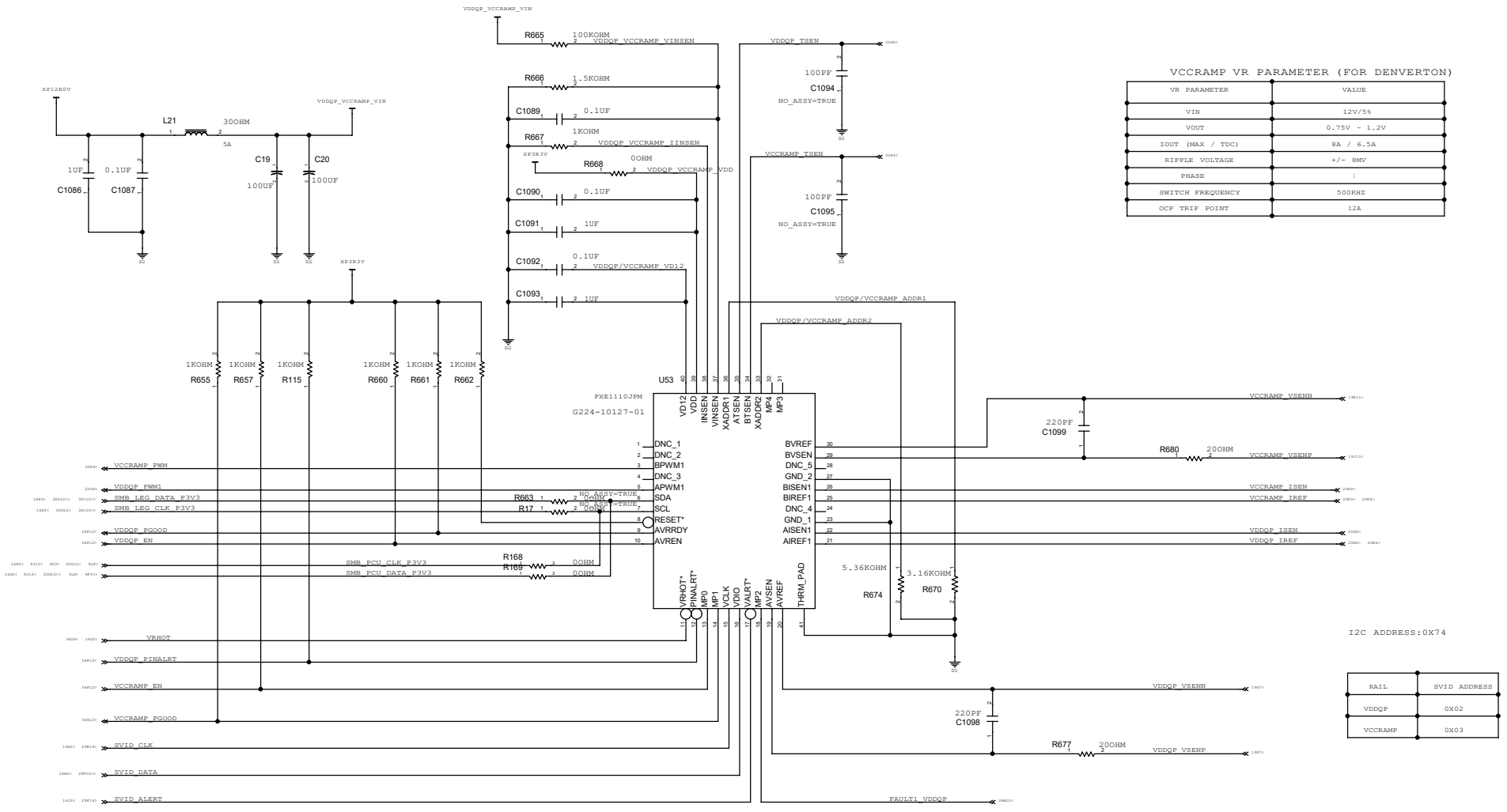
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VIN		3.3		V
VOUT		1.05		V
ICC (MAX)			12.2	A
ICC (TDC)		10.8		A
RIPPLE		+-3		MV



<XP1R05V>

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VCCRAMP VR PARAMETER (FOR DENVERTON)

VR PARAMETER	VALUE
VIN	12V/5%
VOUT	0.75V ~ 1.2V
IOUT (MAX / TDC)	8A / 6.5A
RIPPLE VOLTAGE	+/- 8MV
PHASE	1
SWITCH FREQUENCY	500KHZ
OCP TRIP POINT	12A

I2C ADDRESS:0X74

RAIL	SVID ADDRESS
VDDQP	0X02
VCCRAMP	0X03

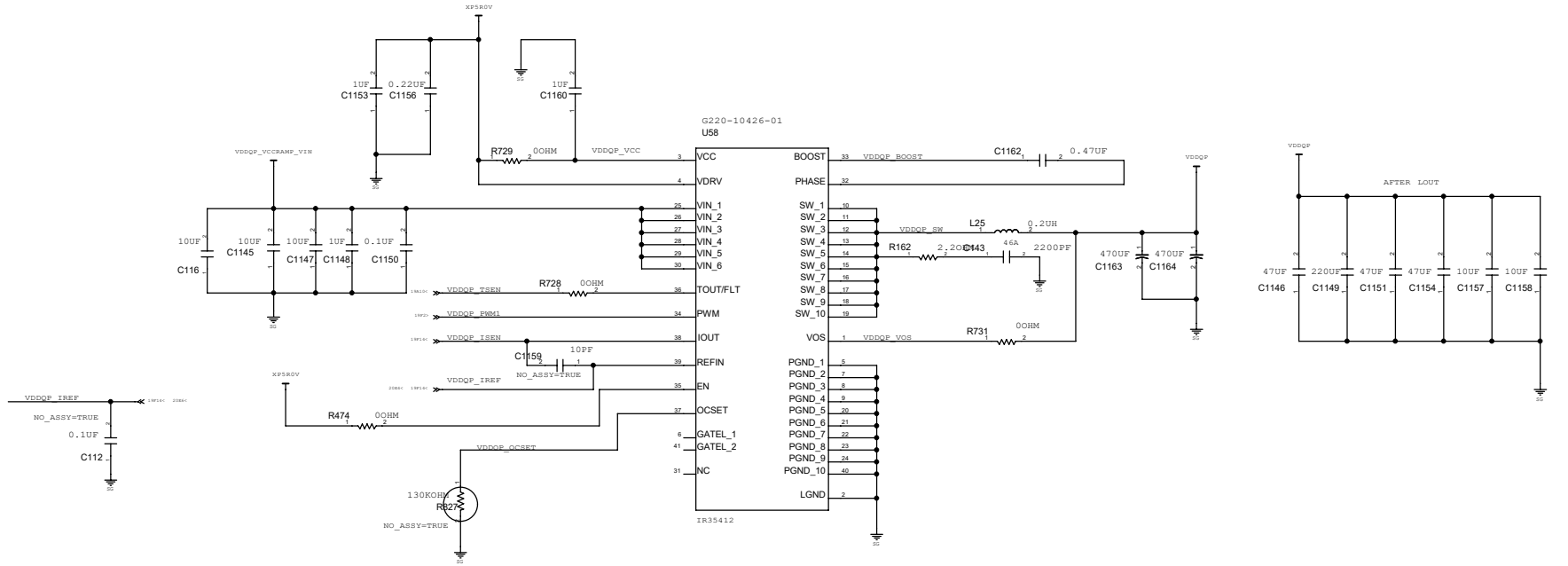
VDDQP VR PARAMETER (FOR SKYLAKE)

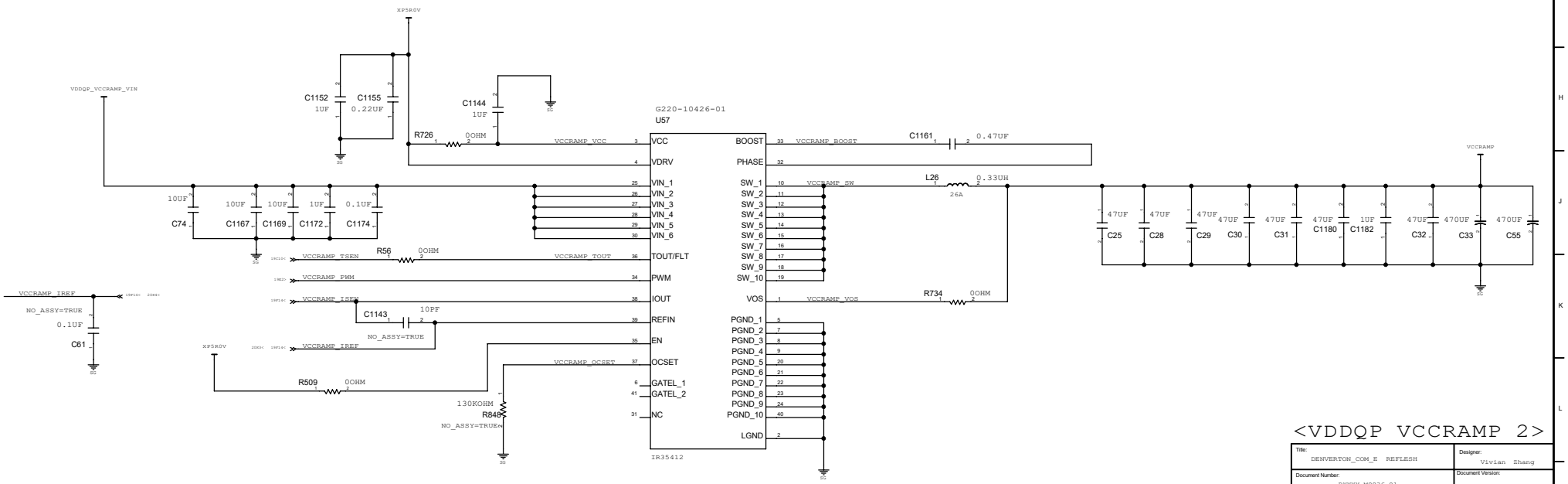
VR PARAMETER	VALUE
VIN	12V/5%
VOUT	1.2V
IOUT (MAX / TDC)	21A / 15A
RIPPLE VOLTAGE	+/- 4MV
PHASE	1
SWITCH FREQUENCY	500KHZ
OCP TRIP POINT	30A

VDDQP VCCRAMP 1

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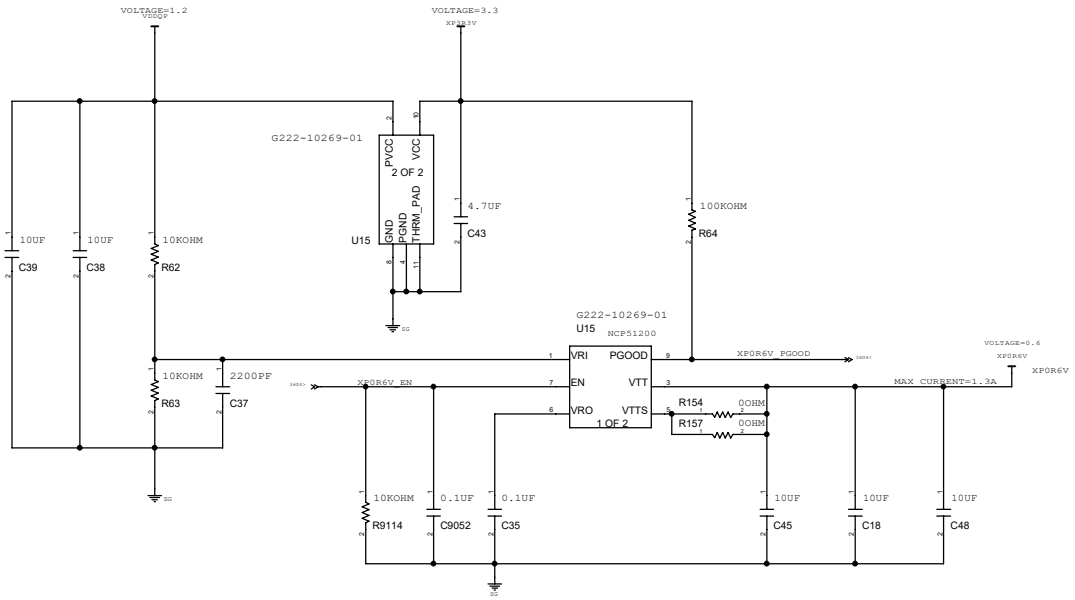




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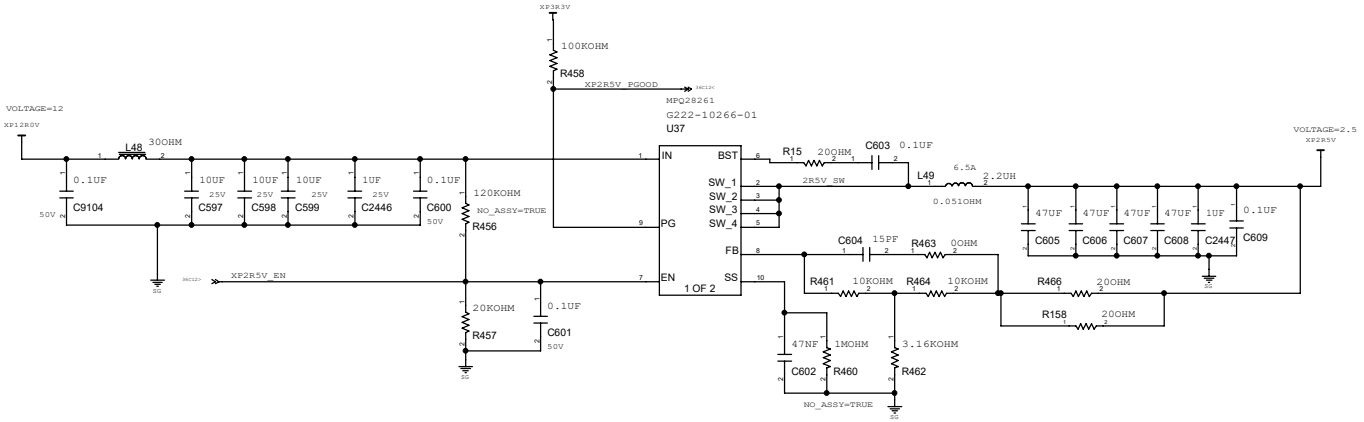
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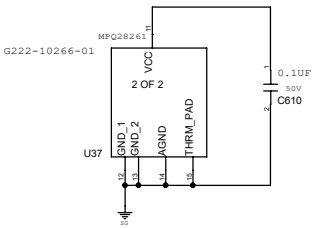


XP0R6V_VTT

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XP2R5V

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M_A_MA<16> 152 RAS*/A16
M_A_MA<15> 156 CAS*/A15
M_A_MA<14> 151 WE*/A14
M_A_MA<13> 158 A13
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M_A_MA<11> 120 A11
M_A_MA<10> 146 A10/AP
M_A_MA<9> 121 A9
M_A_MA<8> 125 A8
M_A_MA<7> 122 A7
M_A_MA<6> 127 A6
M_A_MA<5> 126 A5
M_A_MA<4> 128 A4
M_A_MA<3> 131 A3
M_A_MA<2> 132 A2
M_A_MA<1> 133 A1
M_A_MA<0> 144 A0

M_A_BA<1> 145 BA1
M_A_BA<0> 150 BA0
M_A_BG<1> 113 BG1
M_A_BG<0> 115 BG0

M_A_CLK_DP<1> 138 CK1_T/NF
M_A_CLK_DN<1> 140 CK1_C/NF
M_A_CLK_DP<0> 137 CK0_T
M_A_CLK_DN<0> 139 CK0_C

165 C1/CS3*/NC
M_A_C0 162 C0/CS2*/NC
M_A_CS<1> 157 CS1*
M_A_CS<0> 149 CS0*

M_A_CKE<1> 110 CKE1
M_A_CKE<0> 109 CKE0

M_A_ODT<1> 161 ODT1
M_A_ODT<0> 155 ODT0

M_A_ECC<7> 104 CB7/NC
M_A_ECC<6> 100 CB6/NC
M_A_ECC<5> 87 CB5/NC
M_A_ECC<4> 88 CB4/NC
M_A_ECC<3> 105 CB3/NC
M_A_ECC<2> 101 CB2/NC
M_A_ECC<1> 91 CB1/NC
M_A_ECC<0> 92 CB0/NC

M_A_PAR 143 PARITY
M_AB_RESET_N 108 RESET*
DDR_EVENT_N 134 EVENT*/NF
M_A_ALERT_L 116 ALERT*
M_A_ACT_N 114 ACT*

255 VDDSPD
R21.1 24.7KOHM D0SA2 166 SA2
R23.1 24.7KOHM D0SA1 260 SA1
R24.1 24.7KOHM D0SA0 256 SA0
MEM_DDR_SDA 254 SDA
MEM_DDR_SCL 253 SCL

CPU_DDR_VREFCA 164 VREFCA

96 DM8*/DBI*/NC
241 DM7*/DBI7*
223 DM6*/DBI6*
98 DM5*/DBI5*
178 DM4*/DBI4*
75 DM3*/DBI3*
54 DM2*/DBI2*
33 DM1*/DBI*
12 DM0*/DBI0*

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DQ1 7 M_A_DQ<1>
DQ0 8 M_A_DQ<0>

VOLTAGE=2.5
XP25V
0.1UF C121 A0
C137 0.01UF
VDDQP
1KOHM R423
CPU_DDR_VREFCA
1KOHM R424

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DQS8_T 97 M_A_DQS_DP<8>
DQS8_C 95 M_A_DQS_DN<8>
DQS7_T 242 M_A_DQS_DP<7>
DQS7_C 240 M_A_DQS_DN<7>
DQS6_T 221 M_A_DQS_DP<6>
DQS6_C 219 M_A_DQS_DN<6>
DQS5_T 200 M_A_DQS_DP<5>
DQS5_C 198 M_A_DQS_DN<5>
DQS4_T 179 M_A_DQS_DP<4>
DQS4_C 177 M_A_DQS_DN<4>
DQS3_T 76 M_A_DQS_DP<3>
DQS3_C 74 M_A_DQS_DN<3>
DQS2_T 55 M_A_DQS_DP<2>
DQS2_C 53 M_A_DQS_DN<2>
DQS1_T 34 M_A_DQS_DP<1>
DQS1_C 32 M_A_DQS_DN<1>
DQS0_T 13 M_A_DQS_DP<0>
DQS0_C 11 M_A_DQS_DN<0>
2 OF 4

VOLTAGE=2.5
XP25V
C124 22UF
C127 10UF
C130 0.1UF
C133 0.1UF

VOLTAGE=0.6
XP06V
C136 22UF
C141 0.1UF

VOLTAGE=1.2
VDDQP
C144 22UF
C147 22UF
C56 10UF
C58 10UF
C62 10UF
C111 10UF
C114 10UF
C117 10UF
C120 10UF
C65 10UF
C150 10UF
C69 10UF
C72 10UF
C102 10UF
C153 0.1UF
C156 0.1UF
C159 0.1UF
C107 0.1UF
C101 47UF
C105 47UF
C108 47UF

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98 VSS_47
94 VSS_46
93 VSS_45
90 VSS_44
89 VSS_43
86 VSS_42
85 VSS_41
82 VSS_40
81 VSS_39
78 VSS_38
77 VSS_37
73 VSS_36
72 VSS_35
69 VSS_34
68 VSS_33
65 VSS_32
64 VSS_31
61 VSS_30
60 VSS_29
57 VSS_28
56 VSS_27
52 VSS_26
51 VSS_25
48 VSS_24
47 VSS_23
44 VSS_22
43 VSS_21
40 VSS_20
39 VSS_19
36 VSS_18
35 VSS_17
31 VSS_16
30 VSS_15
27 VSS_14
26 VSS_13
23 VSS_12
22 VSS_11
19 VSS_10
18 VSS_9
15 VSS_8
14 VSS_7
10 VSS_6
9 VSS_5
6 VSS_4
5 VSS_3
2 VSS_2
1 VSS_1
3 OF 4

VSS_94 252
VSS_93 251
VSS_92 248
VSS_91 247
VSS_90 244
VSS_89 243
VSS_88 239
VSS_87 238
VSS_86 235
VSS_85 234
VSS_84 231
VSS_83 230
VSS_82 227
VSS_81 226
VSS_80 223
VSS_79 222
VSS_78 218
VSS_77 217
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VSS_75 213
VSS_74 210
VSS_73 209
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VSS_71 205
VSS_70 202
VSS_69 201
VSS_68 197
VSS_67 196
VSS_66 193
VSS_65 192
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VSS_56 172
VSS_55 171
VSS_54 168
VSS_53 167
VSS_52 107
VSS_51 106
VSS_50 103
VSS_49 102
VSS_48 99

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VOLTAGE=2.5
XP25V
VPP_2 259
VPP_1 257
VOLTAGE=0.6
XP06V
VTT 258
VOLTAGE=1.2
VDDQP
VDD_19 163
VDD_18 160
VDD_17 159
VDD_16 154
VDD_15 153
VDD_14 148
VDD_13 147
VDD_12 142
VDD_11 141
VDD_10 136
VDD_9 135
VDD_8 130
VDD_7 129
VDD_6 124
VDD_5 123
VDD_4 118
VDD_3 117
VDD_2 112
VDD_1 111
G1 G1
G2 G2
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CH0_SODIMM0

Title: DENVERTON_COM_E REFLESH	Designer: Vivian Zhang
Document Number: RXXXX-M0036-01	Document Version: 2.0
Assembly P/N: RXXXX-G0001-01	Date: 2021-04-27
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USE PURSUANT TO COMPANY INSTRUCTIONS

G200-12422-01
J10

RAS*/A16
CAS*/A15
WE*/A14
A13
A12
A11
A10/AP
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0

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BG1
BG0

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M_B_BG<1>
M_B_BG<0>

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CK1_C/NF
CK0_T
CK0_C

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M_B_CLK_DN<1>
M_B_CLK_DP<0>
M_B_CLK_DN<0>

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C0/CS2*/NC
CS1*
CS0*

M_B_C0
M_B_CS<1>
M_B_CS<0>

CKE1
CKE0

M_B_CKE<1>
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ODT1
ODT0

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CB7/NC
CB6/NC
CB5/NC
CB4/NC
CB3/NC
CB2/NC
CB1/NC
CB0/NC

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PARITY
RESET*
EVENT*/NF
ALERT*
ACT*

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M_B_ALERT_L
M_B_ACT_N

VDDSPD
SA2
SA1
SA0
SDA
SCL

MEM_DDR_SDA
MEM_DDR_SCL

VREFCA

DM8*/DBI*/NC
DM7*/DBI7*
DM6*/DBI6*
DM5*/DBI5*
DM4*/DBI4*
DM3*/DBI3*
DM2*/DBI2*
DM1*/DBI*
DM0*/DBI0*

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R1259 1 2 0OHM
DDR_EVENT_N

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XP2R5V
C2042 0.1UF
R36 2.4.7KOHM_DISA2
R37 2.4.7KOHM_DISA1
R51 2.4.7KOHM_DISA0

CPU_DDR_VREFCA
C3012 0.01UF

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J10

DQS8_T M_B_DQS_DP<8>
DQS8_C M_B_DQS_DN<8>
DQS7_T M_B_DQS_DP<7>
DQS7_C M_B_DQS_DN<7>
DQS6_T M_B_DQS_DP<6>
DQS6_C M_B_DQS_DN<6>
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DQS5_C M_B_DQS_DN<5>
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DQS4_C M_B_DQS_DN<4>
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DQS3_C M_B_DQS_DN<3>
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DQS2_C M_B_DQS_DN<2>
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DQS1_C M_B_DQS_DN<1>
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DQS0_C M_B_DQS_DN<0>

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VOLTAGE=2.5
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C63 22UF
C64 10UF
C66 0.1UF
C67 0.1UF

VOLTAGE=0.6
XP0R6V
C68 22UF
C70 0.1UF

VOLTAGE=1.2
VTTDP
C71 22UF
C73 22UF
C75 10UF
C76 10UF
C77 10UF
C78 10UF
C79 10UF
C80 10UF
C81 10UF
C2000 10UF
C82 10UF
C2010 10UF
C2011 10UF
C2014 10UF
C83 0.1UF
C84 0.1UF
C85 0.1UF
C2015 0.1UF
C49 47UF
C88 47UF

VOLTAGE=3.3
XP3R3V
10KOHM R2105
IRQ_DIMM_EVENT_L

VOLTAGE=2.5
XP2R5V
10KOHM R2101
R241 1KOHM
G120-10023-01 Q13
SST3904T116

VOLTAGE=2.5
XP2R5V
10KOHM R69
R75 1KOHM
DDR_EVENT_N
SST3904T116
G120-10023-01 Q12

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J10

VSS_47 VSS_94
VSS_46 VSS_93
VSS_45 VSS_92
VSS_44 VSS_91
VSS_43 VSS_90
VSS_42 VSS_89
VSS_41 VSS_88
VSS_40 VSS_87
VSS_39 VSS_86
VSS_38 VSS_85
VSS_37 VSS_84
VSS_36 VSS_83
VSS_35 VSS_82
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VSS_20 VSS_67
VSS_19 VSS_66
VSS_18 VSS_65
VSS_17 VSS_64
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VSS_15 VSS_62
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VSS_6 VSS_53
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VSS_3 VSS_50
VSS_2 VSS_49
VSS_1 VSS_48

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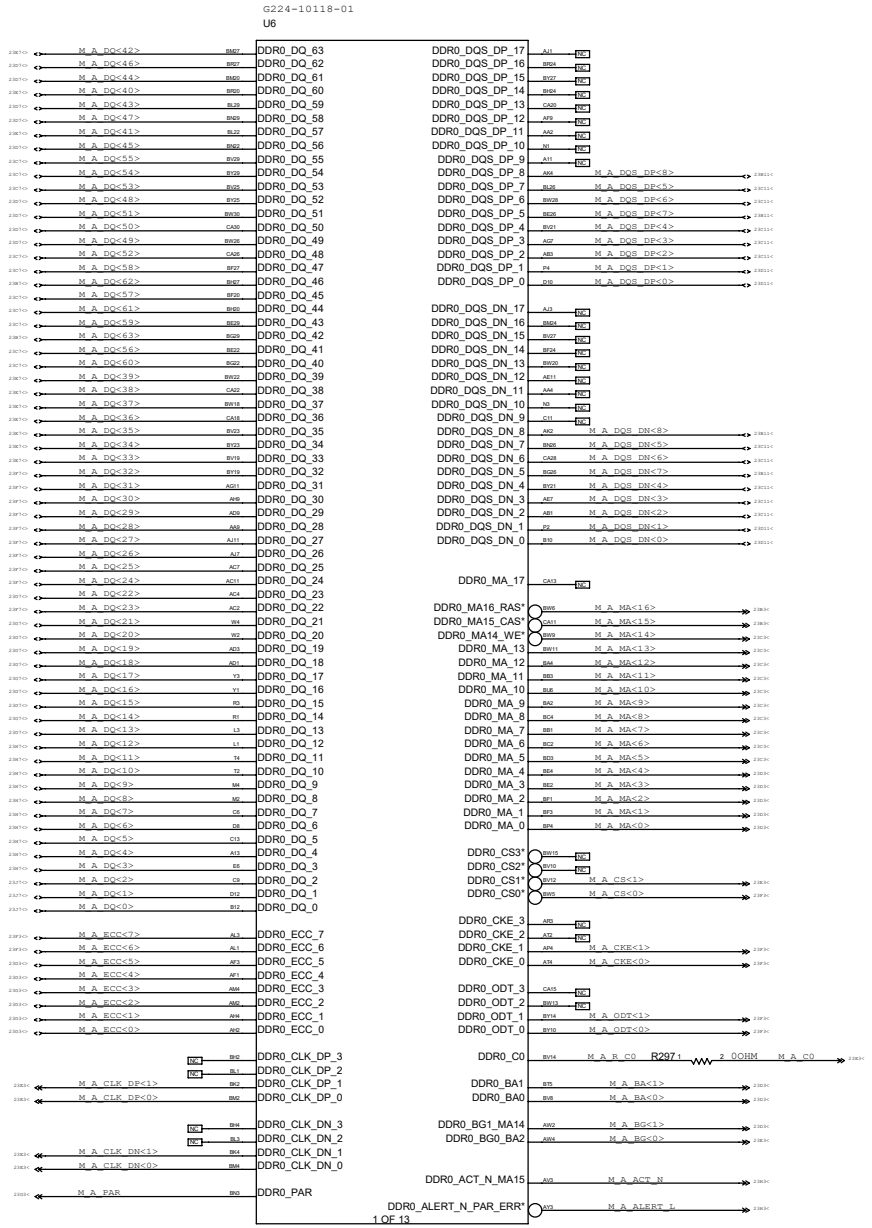
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VOLTAGE=0.6
XP0R6V
VOLTAGE=1.2
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VPP_1
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VDD_18
VDD_17
VDD_16
VDD_15
VDD_14
VDD_13
VDD_12
VDD_11
VDD_10
VDD_9
VDD_8
VDD_7
VDD_6
VDD_5
VDD_4
VDD_3
VDD_2
VDD_1
G1
G2

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CH1_SODIMM1

Title: DENVERTON_COM_E REFLESH	Designer: Vivian Zhang
Document Number: RXXXX-M0036-01	Document Version: 2.0
Assembly P/N: RXXXX-G0001-01	Date: 2021-04-27
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CPU DDR4 CH0

CPU DDR4 CH0

Title: DENVERTON_COM_E REFLESH	Designer: Vivian Zhang
Document Number: RXXXX-M0036-01	Document Version: 2.0
Assembly P/N: RXXXX-G0001-01	Date: 2021-04-27
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U6

M_B_DQ<63>	BN55	DDR1_DQ_63	DDR1_DQS_DP_17	B19			
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M_B_DQ<61>	BH53	DDR1_DQ_61	DDR1_DQS_DP_15	BG11			
M_B_DQ<60>	BG55	DDR1_DQ_60	DDR1_DQS_DP_14	AW13			
M_B_DQ<59>	BR17	DDR1_DQ_59	DDR1_DQS_DP_13	AU8			
M_B_DQ<58>	BM17	DDR1_DQ_58	DDR1_DQS_DP_12	A26			
M_B_DQ<57>	BK17	DDR1_DQ_57	DDR1_DQS_DP_11	H24			
M_B_DQ<56>	BH17	DDR1_DQ_56	DDR1_DQS_DP_10	F24			
M_B_DQ<55>	BM9	DDR1_DQ_55	DDR1_DQS_DP_9	B33			
M_B_DQ<54>	BN7	DDR1_DQ_54	DDR1_DQS_DP_8	C19	M_B_DQS_DP<8>		
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M_B_DQ<46>	BA17	DDR1_DQ_46	DDR1_DQS_DP_0	C32	M_B_DQS_DP<0>		
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M_B_DQ<41>	AR7	DDR1_DQ_44	DDR1_DQS_DN_17	D19			
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M_B_DQ<42>	BD17	DDR1_DQ_42	DDR1_DQS_DN_15	BE11			
M_B_DQ<44>	AU7	DDR1_DQ_41	DDR1_DQS_DN_14	AU13			
M_B_DQ<40>	AT15	DDR1_DQ_40	DDR1_DQS_DN_13	AT11			
M_B_DQ<39>	AV11	DDR1_DQ_39	DDR1_DQS_DN_12	C25			
M_B_DQ<34>	AW9	DDR1_DQ_38	DDR1_DQS_DN_11	K24			
M_B_DQ<32>	AR9	DDR1_DQ_37	DDR1_DQS_DN_10	U24			
M_B_DQ<37>	AN9	DDR1_DQ_36	DDR1_DQS_DN_9	D33			
M_B_DQ<35>	AY11	DDR1_DQ_35	DDR1_DQS_DN_8	A19	M_B_DQS_DN<8>		
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M_B_DQ<33>	AP7	DDR1_DQ_33	DDR1_DQS_DN_6	BL7	M_B_DQS_DN<6>		
M_B_DQ<36>	AP11	DDR1_DQ_32	DDR1_DQS_DN_5	AW17	M_B_DQS_DN<5>		
M_B_DQ<31>	C24	DDR1_DQ_31	DDR1_DQS_DN_4	AT7	M_B_DQS_DN<4>		
M_B_DQ<30>	A24	DDR1_DQ_30	DDR1_DQS_DN_3	B25	M_B_DQS_DN<3>		
M_B_DQ<28>	C28	DDR1_DQ_29	DDR1_DQS_DN_2	G22	M_B_DQS_DN<2>		
M_B_DQ<29>	A28	DDR1_DQ_28	DDR1_DQS_DN_1	P22	M_B_DQS_DN<1>		
M_B_DQ<27>	D23	DDR1_DQ_27	DDR1_DQS_DN_0	A32	M_B_DQS_DN<0>		
M_B_DQ<26>	B23	DDR1_DQ_26					
M_B_DQ<25>	D27	DDR1_DQ_25					
M_B_DQ<24>	B27	DDR1_DQ_24	DDR1_MA_17	AG15			
M_B_DQ<23>	K20	DDR1_DQ_23					
M_B_DQ<22>	H20	DDR1_DQ_22	DDR1_MA16_RAS*	AC22	M_B_MA<16>		
M_B_DQ<21>	K27	DDR1_DQ_21	DDR1_MA15_CAS*	AT22	M_B_MA<15>		
M_B_DQ<20>	H27	DDR1_DQ_20	DDR1_MA14_WE*	AR20	M_B_MA<14>		
M_B_DQ<19>	J18	DDR1_DQ_19	DDR1_MA_13	AW20	M_B_MA<13>		
M_B_DQ<18>	G18	DDR1_DQ_18	DDR1_MA_12	G11	M_B_MA<12>		
M_B_DQ<17>	J26	DDR1_DQ_17	DDR1_MA_11	J7	M_B_MA<11>		
M_B_DQ<16>	G26	DDR1_DQ_16	DDR1_MA_10	AF20	M_B_MA<10>		
M_B_DQ<15>	U20	DDR1_DQ_15	DDR1_MA_9	J11	M_B_MA<9>		
M_B_DQ<14>	R20	DDR1_DQ_14	DDR1_MA_8	R9	M_B_MA<8>		
M_B_DQ<12>	U27	DDR1_DQ_13	DDR1_MA_7	N9	M_B_MA<7>		
M_B_DQ<13>	R27	DDR1_DQ_12	DDR1_MA_6	M7	M_B_MA<6>		
M_B_DQ<11>	T18	DDR1_DQ_11	DDR1_MA_5	N13	M_B_MA<5>		
M_B_DQ<10>	P18	DDR1_DQ_10	DDR1_MA_4	R13	M_B_MA<4>		
M_B_DQ<9>	T26	DDR1_DQ_9	DDR1_MA_3	P7	M_B_MA<3>		
M_B_DQ<8>	P26	DDR1_DQ_8	DDR1_MA_2	T7	M_B_MA<2>		
M_B_DQ<6>	D31	DDR1_DQ_7	DDR1_MA_1	U9	M_B_MA<1>		
M_B_DQ<7>	B31	DDR1_DQ_6	DDR1_MA_0	AR22	M_B_MA<0>		
M_B_DQ<5>	D35	DDR1_DQ_5					
M_B_DQ<4>	B35	DDR1_DQ_4	DDR1_CS3*	AW17			
M_B_DQ<3>	C30	DDR1_DQ_3	DDR1_CS2*	AP17			
M_B_DQ<2>	A30	DDR1_DQ_2	DDR1_CS1*	AV22	M_B_CS<1>		
M_B_DQ<1>	C34	DDR1_DQ_1	DDR1_CS0*	AV22	M_B_CS<0>		
M_B_DQ<0>	A34	DDR1_DQ_0					
			DDR1_CKE_3	G13			
M_B_ECC<7>	D16	DDR1_ECC_7	DDR1_CKE_2	H13			
M_B_ECC<6>	B16	DDR1_ECC_6	DDR1_CKE_1	J15	M_B_CKE<1>		
M_B_ECC<5>	D21	DDR1_ECC_5	DDR1_CKE_0	K13	M_B_CKE<0>		
M_B_ECC<4>	B21	DDR1_ECC_4					
M_B_ECC<3>	C15	DDR1_ECC_3	DDR1_ODT_3	AK17			
M_B_ECC<2>	A15	DDR1_ECC_2	DDR1_ODT_2	AE15			
M_B_ECC<1>	C20	DDR1_ECC_1	DDR1_ODT_1	AT22	M_B_ODT<1>		
M_B_ECC<0>	A20	DDR1_ECC_0	DDR1_ODT_0	AL20	M_B_ODT<0>		
NC	T15	DDR1_CLK_DP_3	DDR1_C0	AJ15	M_B_C0	R298 1	2 0OHM M_B_C0
NC	W17	DDR1_CLK_DP_2					
M_B_CLK_DP<1>	AA17	DDR1_CLK_DP_1	DDR1_BA1	AA20	M_B_BA<1>		
M_B_CLK_DP<0>	AD17	DDR1_CLK_DP_0	DDR1_BA0	AD20	M_B_BA<0>		
NC	U13	DDR1_CLK_DN_3	DDR1_BG1_MA14	J5	M_B_BG<1>		
NC	V15	DDR1_CLK_DN_2	DDR1_BG0_BA2	G7	M_B_BG<0>		
M_B_CLK_DN<1>	Y15	DDR1_CLK_DN_1					
M_B_CLK_DN<0>	AC15	DDR1_CLK_DN_0					
			DDR1_ACT_N_MA15	H9	M_B_ACT_N		
M_B_PAR	V7	DDR1_PAR					
			DDR1_ALERT_N_PAR_ERR*	M15	M_B_ALERT_L		

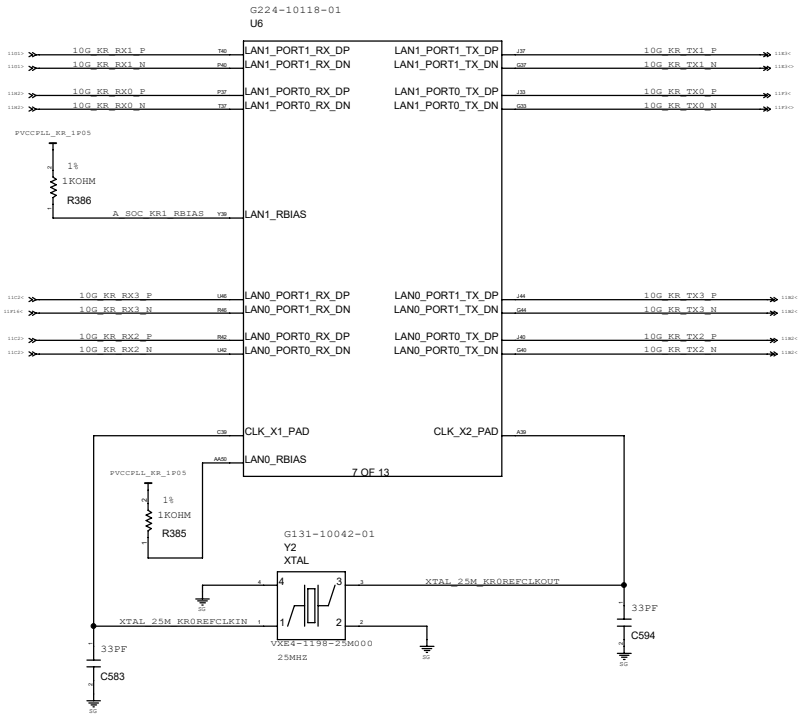
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CPU DDR4 CH1

CPU DDR4 CH1

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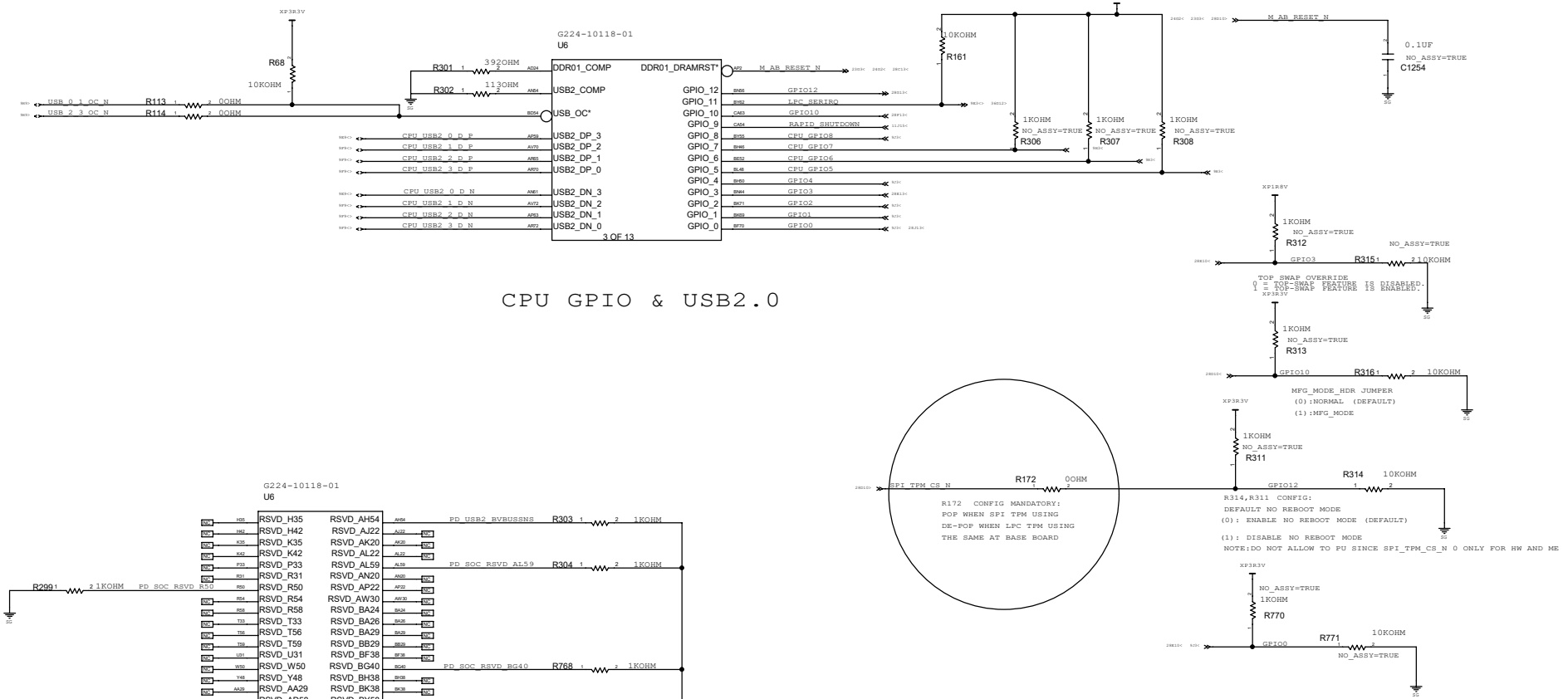
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CPU_10G KR

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CPU GPIO & USB2.0

CPU RESERVE PIN

CPU USB2&GPIO

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G131-10058-01
Y1
XTAL
XTAL_BRTCX2
XTAL_BRTCX1
R317 1MOHM
18PF C573
18PF C574

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RTC_X2_PAD
RTC_X1_PAD
BVCCRTC_EXTPAD
C575 0.1UF
R331 10KOHM
FD_ADR_TRIGGER
ADR_TRIGGER

XP3R3V
R83 2.2KOHM
R84 2.2KOHM
R326 4.7KOHM
R329 4.7KOHM
LAN0_PORT1_I2C_CLK
LAN0_PORT1_I2C_DATA
LAN0_PORT0_I2C_CLK
LAN0_PORT0_I2C_DATA

R1343 4.7KOHM LAN1_PORT0_LED1
R1344 4.7KOHM LAN1_PORT0_LED0
R1345 4.7KOHM LAN0_PORT1_LED1
R1346 4.7KOHM LAN0_PORT1_LED0
R1348 4.7KOHM LAN0_PORT0_LED0

LAN1_PORT0_LED1
LAN1_PORT0_LED0
LAN0_PORT1_LED1
LAN0_PORT1_LED0
LAN1_PORT1_I2C_DATA
LAN1_PORT0_I2C_DATA
LAN1_PORT0_I2C_CLK
GPIO38
LAN0_PORT0_LED1
LAN0_PORT0_LED0
LAN1_PORT1_I2C_CLK
LAN1_PORT0_I2C_CLK
R11 10KOHM PU_SUSPWRDNACK
SUSPWRDNACK
CPLD_COREPWROK
COREPWROK
R774 1KOHM

XP1R05V
R85 49.9OHM CX_PRDY*
R102 49.9OHM CX_PREQ*
R14 1KOHM CTBTRIGOUT
R101 1KOHM CTBTRIGINOUT

NCSI_RXD_1
NCSI_RXD_0
NCSI_CLK_IN
NCSI_RXD1
NCSI_RXD0
NCSI_CLK_IN

SPI_CLK
SPI_CS1*
SPI_CS0*
SPI_IO_3
SPI_IO_2
SPI_MISO_IO_1
SPI_MOSI_IO_0
ESPI_ALRT*
ESPI_CLK
ESPI_CS*
ESPI_IO_3
ESPI_IO_2
ESPI_IO_1
ESPI_IO_0
ESPI_RST*
SVID_CLK
SVID_DATA
SVID_ALERT*
RTEST*
SRTCRST*
SUS_STAT*
MEMHOT*
THERMTRIP*
TCK
TDI
TDO
TMS
TRST*
SATA1_LED*
SATA0_LED*
SATA1_SDOUT
SATA0_SDOUT
SATA_PDETECT_1
SATA_PDETECT_0
UART1_TXD
UART1_RXD
UART0_TXD
UART0_RXD
NCSI_TXD_1
NCSI_TXD_0
NCSI_TX_EN
NCSI_CRS_DV
NCSI_ARB_IN
NCSI_ARB_OUT
ESPI_IRCOMP

SPI_CLK
SPI_CS1
SPI_CS0
SPI_IO3
SPI_IO2
SPI_MISO
SPI_MOSI
LPC_CLKRUN_N
LPC_CLK
LPC_FRAME_N
LPC_AD<3>
LPC_AD<2>
LPC_AD<1>
LPC_AD<0>
GPIO70
SVID_CLK
SVID_DATA
SVID_ALERT
RTC_RTEST_N
RST_SRTCRST_N
SUS_STAT_N
MEMHOT_N
THERMTRIP_N
JTAG_TCK_CPU
JTAG_TDI_CPU
JTAG_TDO_CPU
JTAG_TMS_CPU
JTAG_TRST_CPU
SATA0_LED_N
UART1_R_TXD
UART0_R_TXD
NCSI_TXD_1
NCSI_TXD_0
NCSI_TX_EN
NCSI_CRS_DV
NCSI_ARB_IN
NCSI_ARB_OUT
ESPI_IRCOMP

R341 0OHM LPC_R_CLK
R12 0OHM LPC_R_LAD3
R13 0OHM LPC_R_LAD2
R344 0OHM LPC_R_LAD1
R345 0OHM LPC_R_LAD0
R332 0OHM SVID_R_CLK
R333 0OHM SVID_R_DATA
R334 200OHM SVID_R_ALERT
R86 0OHM
R111 10KOHM
R335 0OHM UART1_R_TXD
R775 0OHM UART0_R_TXD
R348 100OHM

XP3R3V
R129 4.7KOHM

XP1R05V
PLACE AT REMOTE END
PLACE AT REMOTE END
PLACE AT NEAR END
PLACE AT NEAR END
R351 40.2OHM
R352 120OHM
R87 120OHM
R354 49.9OHM

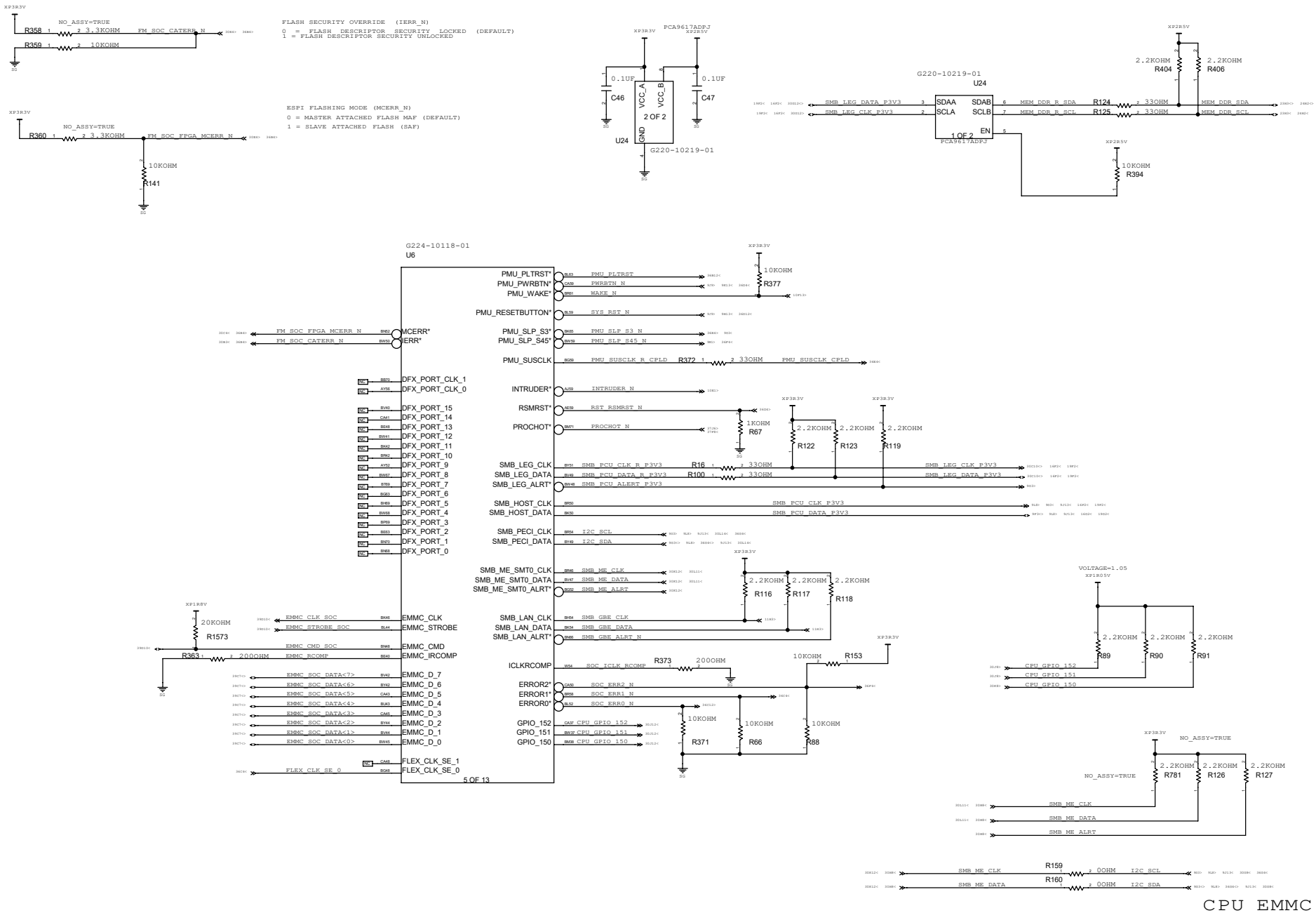
P3V_BAT
RTC_RTEST_N
RST_SRTCRST_N
R76 15KOHM
R776 15KOHM
C42 1UF
C44 1UF
PUT IT ON TOP SIDE
PUT IT ON TOP SIDE

XP1R05V 1.05
R3301 49.9OHM JTAG_TMS_CPU
R3302 49.9OHM JTAG_TDI_CPU
R3303 49.9OHM JTAG_TDO_CPU
R232 1KOHM JTAG_TCK_CPU
R233 1KOHM JTAG_TRST_CPU

CPU/PCH MISC

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CPU EMMC I2C

CPU EMMC_SMB

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U6

FROM USB3.0	USB_SSRX0_P	AMF2	HSIO_RX_DP_19	HSIO_TX_DP_19	AK65	USB_SSTX0_P	TO USB3.0
	USB_SSRX1_P	AL72	HSIO_RX_DP_18	HSIO_TX_DP_18	AH65	USB_SSTX1_P	
FROM SATA	SATA1_RX_P	AJ72	HSIO_RX_DP_17	HSIO_TX_DP_17	AF65	SATA1_TX_P	TO SATA
	SATA0_RX_P	AF72	HSIO_RX_DP_16	HSIO_TX_DP_16	AD65	SATA0_TX_P	
	CPU_PCIE15_RX_P	AD72	HSIO_RX_DP_15	HSIO_TX_DP_15	AA65	CPU_PCIE15_TX_P	
	CPU_PCIE14_RX_P	AB72	HSIO_RX_DP_14	HSIO_TX_DP_14	W65	CPU_PCIE14_TX_P	
FROM COM_E CONNECTOR	CPU_PCIE13_RX_P	Y72	HSIO_RX_DP_13	HSIO_TX_DP_13	U65	CPU_PCIE13_TX_P	TO COME CONNECTOR
	CPU_PCIE12_RX_P	V72	HSIO_RX_DP_12	HSIO_TX_DP_12	R65	CPU_PCIE12_TX_P	
	CPU_PCIE11_RX_P	R72	HSIO_RX_DP_11	HSIO_TX_DP_11	N65	CPU_PCIE11_TX_P	
	CPU_PCIE10_RX_P	N72	HSIO_RX_DP_10	HSIO_TX_DP_10	K65	CPU_PCIE10_TX_P	
	CPU_PCIE9_RX_P	L72	HSIO_RX_DP_9	HSIO_TX_DP_9	H65	CPU_PCIE9_TX_P	
	CPU_PCIE8_RX_P	J70	HSIO_RX_DP_8	HSIO_TX_DP_8	GB3	CPU_PCIE8_TX_P	
	CPU_PCIE7_RX_P	G67	HSIO_RX_DP_7	HSIO_TX_DP_7	G59	CPU_PCIE7_TX_P	
	CPU_PCIE6_RX_P	G67	HSIO_RX_DP_6	HSIO_TX_DP_6	M59	CPU_PCIE6_TX_P	
	CPU_PCIE5_RX_P	AB3	HSIO_RX_DP_5	HSIO_TX_DP_5	M56	CPU_PCIE5_TX_P	
FROM COM_E CONNECTOR	CPU_PCIE4_RX_P	AB1	HSIO_RX_DP_4	HSIO_TX_DP_4	J56	CPU_PCIE4_TX_P	
	CPU_PCIE3_RX_P	AS9	HSIO_RX_DP_3	HSIO_TX_DP_3	GS2	CPU_PCIE3_TX_P	TO COME CONNECTOR
	CPU_PCIE2_RX_P	AS7	HSIO_RX_DP_2	HSIO_TX_DP_2	M52	CPU_PCIE2_TX_P	
	CPU_PCIE1_RX_P	AS4	HSIO_RX_DP_1	HSIO_TX_DP_1	M48	CPU_PCIE1_TX_P	
	CPU_PCIE0_RX_P	AS2	HSIO_RX_DP_0	HSIO_TX_DP_0	J48	CPU_PCIE0_TX_P	

FROM USB3.0	USB_SSRX0_N	AMF0	HSIO_RX_DN_19	HSIO_TX_DN_19	AL66	USB_SSTX0_N	TO USB3.0
	USB_SSRX1_N	AL70	HSIO_RX_DN_18	HSIO_TX_DN_18	AJ63	USB_SSTX1_N	
FROM SATA	SATA1_RX_N	AJ70	HSIO_RX_DN_17	HSIO_TX_DN_17	AG66	SATA1_TX_N	TO SATA
	SATA0_RX_N	AF70	HSIO_RX_DN_16	HSIO_TX_DN_16	AE63	SATA0_TX_N	
	CPU_PCIE15_RX_N	AD70	HSIO_RX_DN_15	HSIO_TX_DN_15	AC66	CPU_PCIE15_TX_N	
	CPU_PCIE14_RX_N	AB70	HSIO_RX_DN_14	HSIO_TX_DN_14	Y63	CPU_PCIE14_TX_N	
FROM COM_E CONNECTOR	CPU_PCIE13_RX_N	Y70	HSIO_RX_DN_13	HSIO_TX_DN_13	V66	CPU_PCIE13_TX_N	TO COME CONNECTOR
	CPU_PCIE12_RX_N	V70	HSIO_RX_DN_12	HSIO_TX_DN_12	T63	CPU_PCIE12_TX_N	
	CPU_PCIE11_RX_N	R70	HSIO_RX_DN_11	HSIO_TX_DN_11	P66	CPU_PCIE11_TX_N	
	CPU_PCIE10_RX_N	N70	HSIO_RX_DN_10	HSIO_TX_DN_10	M63	CPU_PCIE10_TX_N	
	CPU_PCIE9_RX_N	L70	HSIO_RX_DN_9	HSIO_TX_DN_9	J66	CPU_PCIE9_TX_N	
	CPU_PCIE8_RX_N	H69	HSIO_RX_DN_8	HSIO_TX_DN_8	J63	CPU_PCIE8_TX_N	
	CPU_PCIE7_RX_N	F69	HSIO_RX_DN_7	HSIO_TX_DN_7	H61	CPU_PCIE7_TX_N	
	CPU_PCIE6_RX_N	C65	HSIO_RX_DN_6	HSIO_TX_DN_6	J59	CPU_PCIE6_TX_N	
	CPU_PCIE5_RX_N	C63	HSIO_RX_DN_5	HSIO_TX_DN_5	K58	CPU_PCIE5_TX_N	
FROM COM_E CONNECTOR	CPU_PCIE4_RX_N	C61	HSIO_RX_DN_4	HSIO_TX_DN_4	G56	CPU_PCIE4_TX_N	TO COME CONNECTOR
	CPU_PCIE3_RX_N	C59	HSIO_RX_DN_3	HSIO_TX_DN_3	H54	CPU_PCIE3_TX_N	
	CPU_PCIE2_RX_N	C57	HSIO_RX_DN_2	HSIO_TX_DN_2	J52	CPU_PCIE2_TX_N	
	CPU_PCIE1_RX_N	C54	HSIO_RX_DN_1	HSIO_TX_DN_1	K50	CPU_PCIE1_TX_N	
	CPU_PCIE0_RX_N	C52	HSIO_RX_DN_0	HSIO_TX_DN_0	G48	CPU_PCIE0_TX_N	

XP3R3V

10KOHM R387, R388, R389, R390, R59, R60, R61

	PU_PCIE_CLKREQ7_N	BW58	PCIE_CLKREQ7*	CLK_OUT_DP_4	C50	NC	
	PU_PCIE_CLKREQ6_N	BV61	PCIE_CLKREQ6*	CLK_OUT_DP_3	C48	NC	
	PU_PCIE_CLKREQ5_N	BW52	PCIE_CLKREQ5*	CLK_OUT_DP_2	C45	NC	TO I211
36C12>	GPIO45	BC61	PCIE_CLKREQ4*	CLK_OUT_DP_1	C43	NC	
	PU_PCIE_CLKREQ3_N	BJ60	PCIE_CLKREQ3*	CLK_OUT_DP_0	C41	CLK_PCIE_CON_P	TO COME CONNECTOR
	PU_PCIE_CLKREQ2_N	BV51	PCIE_CLKREQ2*				
	PU_PCIE_CLKREQ1_N	BA59	PCIE_CLKREQ1*	CLK_OUT_DN_4	A50	NC	
	PU_PCIE_CLKREQ0_N	AP56	PCIE_CLKREQ0*	CLK_OUT_DN_3	A48	NC	
				CLK_OUT_DN_2	A45	NC	TO I211
				CLK_OUT_DN_1	A43	NC	
				CLK_OUT_DN_0	A41	CLK_PCIE_CON_N	TO COME CONNECTOR

R391 1 2100OHM 2 SOC_COMPREF_DP AD54 HSIO_COMPREF_DP
SOC_COMPREF_DN AC56 HSIO_COMPREF_DN
ROUTE THESE SIGNALS DIFFERENTIALLY

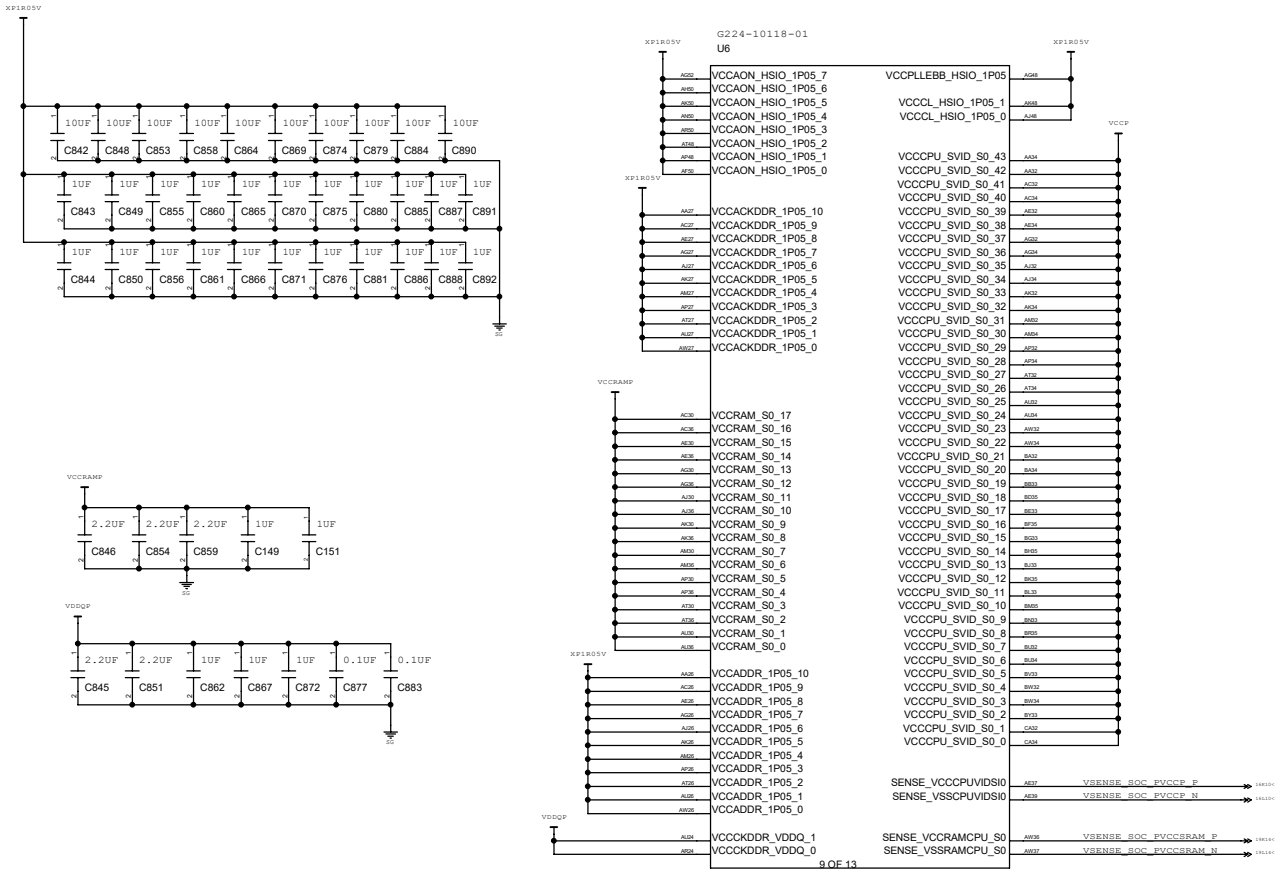
HSHV_IRCOMP BD42 SOC_HSHV_IRCOMP R392 1 2 100OHM

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CPU HSIO

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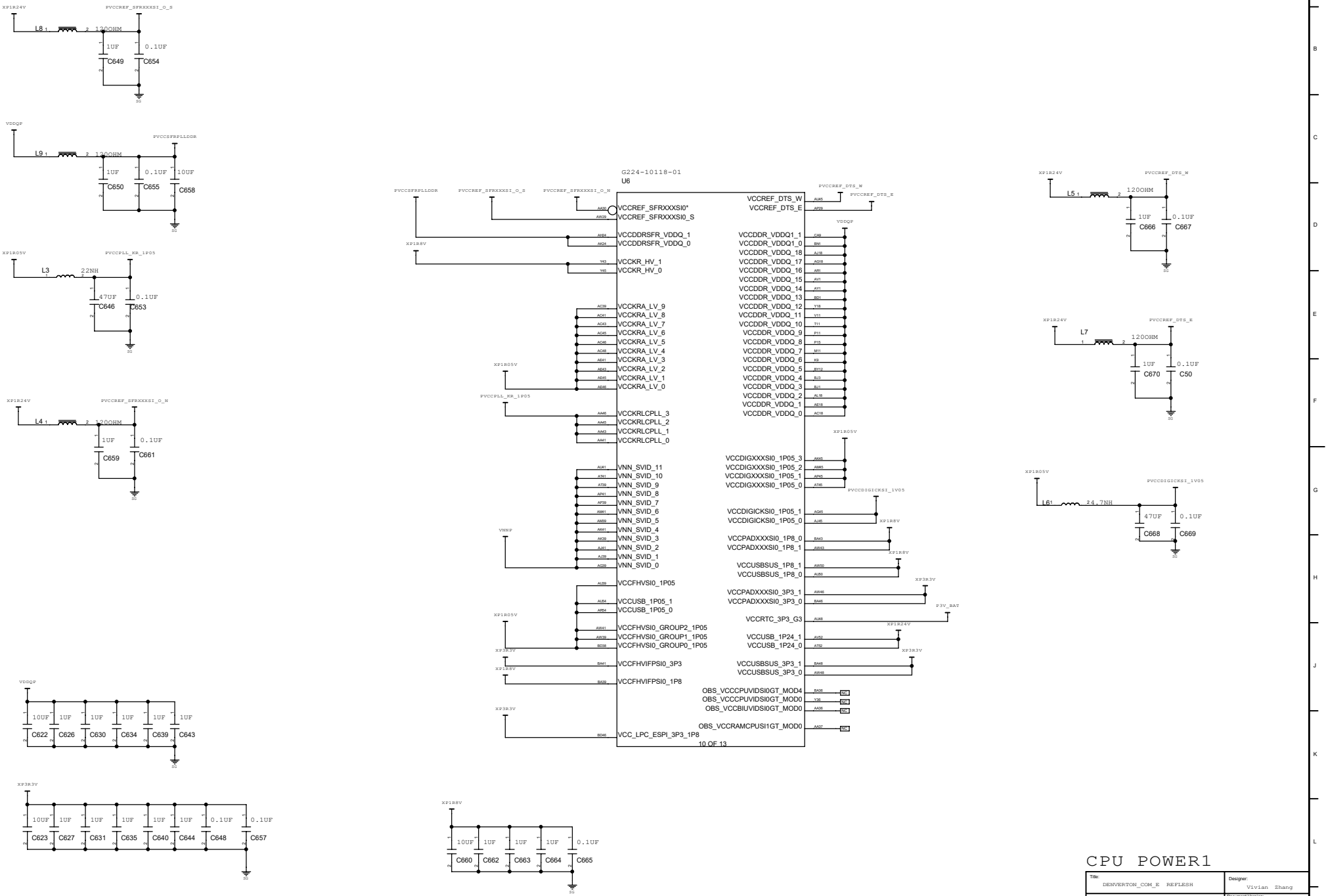
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CPU POWER0

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AG46	VSS_165	VSS_1	A37
AG43	VSS_164	VSS_2	AA39
AV68	VSS_163	VSS_3	AA54
AK61	VSS_162	VSS_4	AA61
AW24	VSS_161	VSS_5	BJ70
BT66	VSS_160	VSS_6	BY50
BJ67	VSS_159	VSS_7	BY53
AK54	VSS_158	VSS_8	BY47
AW58	VSS_157	VSS_9	BY40
AY5	VSS_156	VSS_10	BY35
AY18	VSS_155	VSS_11	BY31
AG41	VSS_154	VSS_12	BY16
AT66	VSS_153	VSS_13	G66
AT69	VSS_152	VSS_14	AC69
AY68	VSS_151	VSS_15	AC71
BA9	VSS_150	VSS_16	BW63
BA13	VSS_149	VSS_17	BW57
D52	VSS_148	VSS_18	H50
BA27	VSS_147	VSS_19	BW43
AT71	VSS_146	VSS_20	BW34
BA30	VSS_145	VSS_21	BV35
AF61	VSS_144	VSS_22	BV31
E67	VSS_143	VSS_23	BV16
AW49	VSS_142	VSS_24	BE71
AW71	VSS_141	VSS_25	AM43
AD50	VSS_140	VSS_26	E37
AF54	VSS_139	VSS_27	BJ55
BB5	VSS_138	VSS_28	BJ61
BB7	VSS_137	VSS_29	BJ59
BB11	VSS_136	VSS_30	BJ54
BB18	VSS_135	VSS_31	BJ52
BB22	VSS_134	VSS_32	BJ48
BB26	VSS_133	VSS_33	BJ45
BC71	VSS_132	VSS_34	BJ41
BB37	VSS_131	VSS_35	BJ39
BB40	VSS_130	VSS_36	BJ37
BB44	VSS_129	VSS_37	BJ30
BB48	VSS_128	VSS_38	BJ28
BB52	VSS_127	VSS_39	BJ26
BB59	VSS_126	VSS_40	BJ24
BB63	VSS_125	VSS_41	BJ22
BB66	VSS_124	VSS_42	BJ20
BD5	VSS_123	VSS_43	BJ18
BD9	VSS_122	VSS_44	BJ15
BD13	VSS_121	VSS_45	BJ13
BD20	VSS_120	VSS_46	BJ11
BD24	VSS_119	VSS_47	E30
BD27	VSS_118	VSS_48	BT8
BD31	VSS_117	VSS_49	E32
BD5	VSS_116	VSS_50	BP36
A22	VSS_115	VSS_51	BP31
AC37	VSS_114	VSS_52	BR6
BD69	VSS_113	VSS_53	CA24
BE7	VSS_112	VSS_54	F6
BE15	VSS_111	VSS_55	BR07
BE18	VSS_110	VSS_56	BN18
BE37	VSS_109	VSS_57	BN11
BF5	VSS_108	VSS_58	BN6
BF13	VSS_107	VSS_59	BM65
BF17	VSS_106	VSS_60	BM61
BF31	VSS_105	VSS_61	BM58
BW65	VSS_104	VSS_62	BM54
BF42	VSS_103	VSS_63	BM50
BF46	VSS_102	VSS_64	BM46
BF50	VSS_101	VSS_65	BM42
BF54	VSS_100	VSS_66	BM31
BF58	VSS_99	VSS_67	BL72
BF61	VSS_98	VSS_68	BL68
BF65	VSS_97	VSS_69	BL37
BF68	VSS_96	VSS_70	BL18
AE66	VSS_95	VSS_71	BL5
AE56	VSS_94	VSS_72	BK31
BG18	VSS_93	VSS_73	BK27
BG37	VSS_92	VSS_74	BK24
BH31	VSS_91	VSS_75	BK20
BJ5	VSS_90	VSS_76	BJ68
BJ11	VSS_89	VSS_77	BJ63
BJ18	VSS_88	VSS_78	BJ59
BJ22	VSS_87	VSS_79	BJ56
BJ26	VSS_86	VSS_80	BJ52
BJ29	VSS_85	VSS_81	BJ48
BJ37	VSS_84	VSS_82	BJ44
BJ40	VSS_83		

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AT43	VSS_332	VSS_166	AK43
R68	VSS_331	VSS_167	AV18
T29	VSS_330	VSS_168	AV5
H31	VSS_329	VSS_169	BM69
AA69	VSS_328	VSS_170	AP43
P56	VSS_327	VSS_171	AL7
D58	VSS_326	VSS_172	AU57
V1	VSS_325	VSS_173	AU29
V3	VSS_324	VSS_174	B60
V5	VSS_323	VSS_175	AT63
V18	VSS_322	VSS_176	AL52
V22	VSS_321	VSS_177	AM71
V25	VSS_320	VSS_178	AJ43
V29	VSS_319	VSS_179	AT37
V44	VSS_318	VSS_180	AT29
V46	VSS_317	VSS_181	AT18
V52	VSS_316	VSS_182	AM69
V56	VSS_315	VSS_183	B58
V59	VSS_314	VSS_184	AR68
V63	VSS_313	VSS_185	AP52
P48	VSS_312	VSS_186	AP69
V68	VSS_311	VSS_187	AN24
AA71	VSS_310	VSS_188	AR5
AD61	VSS_309	VSS_189	AP71
W9	VSS_308	VSS_190	AP45
W13	VSS_307	VSS_191	D29
W20	VSS_306	VSS_192	AP37
W24	VSS_305	VSS_193	D14
P44	VSS_304	VSS_194	AP18
M33	VSS_303	VSS_195	AN68
W61	VSS_302	VSS_196	AN65
K61	VSS_301	VSS_197	AN58
Y5	VSS_300	VSS_198	AR58
Y7	VSS_299	VSS_199	AN57
Y11	VSS_298	VSS_200	AN53
Y22	VSS_297	VSS_201	AN5
Y26	VSS_296	VSS_202	AN3
Y27	VSS_295	VSS_203	AN1
AU43	VSS_294	VSS_204	AM46
Y30	VSS_293	VSS_205	AM37
Y32	VSS_292	VSS_206	AM29
K54	VSS_291	VSS_207	AU68
Y37	VSS_290	VSS_208	AU63
H58	VSS_289	VSS_209	AK71
BA20	VSS_288	VSS_210	K4
J72	VSS_287	VSS_211	AL15
B64	VSS_286	VSS_212	AL11
B51	VSS_285	VSS_213	AR13
Y46	VSS_284	VSS_214	AL5
AE69	VSS_283	VSS_215	AT46
AE71	VSS_282	VSS_216	AT56
D49	VSS_281	VSS_217	AP66
Y66	VSS_280	VSS_218	AK58
AA13	VSS_279	VSS_219	AT39
AA24	VSS_278	VSS_220	AK46
AH61	VSS_277	VSS_221	U37
D47	VSS_276	VSS_222	AK37
AH69	VSS_275	VSS_223	AK29
D44	VSS_274	VSS_224	AK13
AA48	VSS_273	VSS_225	AK9
AA58	VSS_272	VSS_226	AJ58
AB5	VSS_271	VSS_227	AJ56
AB68	VSS_270	VSS_228	AR61
AC29	VSS_269	VSS_229	AW54
AH71	VSS_268	VSS_230	AJ52
AC52	VSS_267	VSS_231	B38
D42	VSS_266	VSS_232	AJ46
AC63	VSS_265	VSS_233	AK69
AW65	VSS_264	VSS_234	AJ37
AW61	VSS_263	VSS_235	AJ29
AD5	VSS_262	VSS_236	AJ5
AD13	VSS_261	VSS_237	B40
AF24	VSS_260	VSS_238	B42
D40	VSS_259	VSS_239	AH13
AD68	VSS_258	VSS_240	AG63
AE2	VSS_257	VSS_241	BA37
AE4	VSS_256	VSS_242	B44
AE29	VSS_255	VSS_243	AG37
D38	VSS_254	VSS_244	AG29
B49	VSS_253	VSS_245	AF68
AE48	VSS_252	VSS_246	AF58
AE52	VSS_251	VSS_247	AM68
B47	VSS_250	VSS_248	AP13
AF5	VSS_249		

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D60	VSS_463	NC_ROT	A70
D55	VSS_462	VSS_ROT	CA3
D53	VSS_461		
Y52	VSS_460	VSS_499	J1
B62	VSS_459	VSS_501	G1
K71	VSS_458	VSS_500	E1
CF2	VSS_457	VSS_504	CA7
BU3	VSS_456	VSS_503	CA66
BR3	VSS_455	VSS_502	C72
K69	VSS_454	VSS_506	C3
F70	VSS_453	VSS_505	BW76
D64	VSS_452	VSS_507	BW3
H38	VSS_451	VSS_508	BW1
R66	VSS_450	VSS_509	BU72
F5	VSS_449	VSS_511	BU1
F3	VSS_448	VSS_510	BR72
E70	VSS_447	VSS_512	BR1
E3	VSS_446	VSS_514	BN72
C66	VSS_445	VSS_513	A9
C5	VSS_444	VSS_516	A7
BA50	VSS_443	VSS_515	A68
AU46	VSS_442	VSS_517	A66
BU70	VSS_441	VSS_519	A60
BR70	VSS_440	VSS_518	A5
E65	VSS_439	VSS_521	BW72
Y41	VSS_438	VSS_520	C70
Y34	VSS_437	VSS_522	CA65
Y29	VSS_436	VSS_523	CA68
V33	VSS_435	VSS_524	CA70
U61	VSS_434	VSS_525	E72
V60	VSS_433		
T71	VSS_432		
T52	VSS_431	VSS_333	W71
J68	VSS_430	VSS_334	BB56
U58	VSS_429	VSS_335	H46
P52	VSS_428	VSS_336	B53
K31	VSS_427	VSS_337	R5
U64	VSS_426	VSS_338	W59
N42	VSS_425	VSS_339	P29
N38	VSS_424	VSS_340	N68
T69	VSS_423	VSS_341	P59
M37	VSS_422	VSS_342	N61
U60	VSS_421	VSS_343	N58
K38	VSS_420	VSS_344	N54
E9	VSS_419	VSS_345	N50
E11	VSS_418	VSS_346	N46
E13	VSS_417	VSS_347	N35
E15	VSS_416	VSS_348	N27
E18	VSS_415	VSS_349	N24
E20	VSS_414	VSS_350	N20
E22	VSS_413	VSS_351	N17
E24	VSS_412	VSS_352	N5
E26	VSS_411	VSS_353	K46
E28	VSS_410	VSS_354	P71
E34	VSS_409	VSS_355	M66
E39	VSS_408	VSS_356	P53
E41	VSS_407	VSS_357	R35
E43	VSS_406	VSS_358	R38
E45	VSS_405	VSS_359	J59
E48	VSS_404	VSS_360	P59
E50	VSS_403	VSS_361	M44
E52	VSS_402	VSS_362	M40
E54	VSS_401	VSS_363	M29
E57	VSS_400	VSS_364	M26
E59	VSS_399	VSS_365	M22
E61	VSS_398	VSS_366	M18
E63	VSS_397	VSS_367	L68
BU50	VSS_396	VSS_368	L5
G6	VSS_395	VSS_369	H4
R17	VSS_394	VSS_370	N31
B14	VSS_393	VSS_371	K17
U58	VSS_392	VSS_372	K2
U55	VSS_391	VSS_373	C37
G29	VSS_390	VSS_374	C22
M69	VSS_389	VSS_375	BA45
D66	VSS_388	VSS_376	B29
D51	VSS_387	VSS_377	T44
MF1	VSS_386	VSS_378	J29
BL9	VSS_385	VSS_379	V37
H67	VSS_384	VSS_380	J3
T66	VSS_383	VSS_486	CA5
T48	VSS_382	VSS_496	Y56
AW45	VSS_381	VSS_497	Y66

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CPU GND

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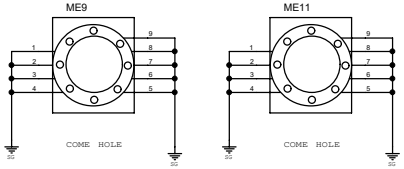
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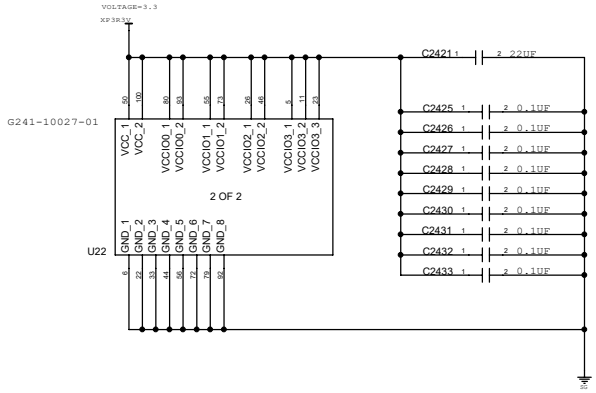
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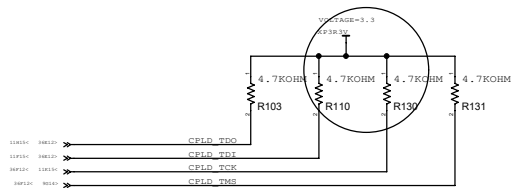
G241-10027-01
U22

LPC_AD<3>	1	PL2C/L_GPLLT_IN_3	PR2A_1	75	PMU_PLTRST
SUS_STAT_N	2	PL2D/L_GPLLC_IN_3	PR2B_1	74	SATA0_LED_N
CPLD_COREPWROK	3	PL3A/PCLKT3_2_3	PR3A_1	71	GPIO70
PM_SOC_FPGA_MCERR_N	4	PL3B/PCLKC3_2_3	PR3B_1	70	IRQ_DIMM_EVENT_L
PM_SOC_CATERR_N	7	PL3C_3			
LPC_AD<2>	8	PL3D_3	PR4A_1	69	FAULT1_VDDQP
			PR4B_1	68	FAULT1_VCCP
FLEX_CLK_SE_0	9	PL4A_3	PR4C_1	67	XP2R5V_PGOOD
XP1R8V_EN	10	PL4B_3	PR4D_1	66	XP2R5V_EN
BIOS_DIS1_N	12	PL5A/PCLKT3_1_3	PR5A_1	65	SLEEP_CPLD_N
SOC_ERR1_N	13	PL5B/PCLKC3_1_3	PR5B_1	64	XP1R24V_EN
LPC_AD<1>	14	PL5C_3	PR5C/PCLKT1_0_1	63	GPIO45
LPC_CLKRUN_N	15	PL5D_3	PR5D/PCLKC1_0_1	62	SOC_ERR0_N
BIOS_SPI_CS0	16	PL8A_3	PR8A_1	61	LPC_CLK
RST_RSMRST_N	17	PL8B_3			
VRHOT	18	PL8C_3	PR8C_1	60	SYS_RST_N
EXCD0_CPPE_N	19	PL8D_3	PR8D_1	59	LPC_AD<0>
	20	PL9A/PCLKT3_0_3	PR9A_1	58	LPC_FRAME_N
PWRBTN_N	21	PL9B/PCLKC3_0_3	PR9B_1	57	EXCD1_CPPE_N
			PR9C_1	54	GPIO38
BIOS_SPI_CS1	24	PL10C_3	PR9D_1	53	CPLD_PROCHOT_L
XP3R3V_PGOOD	25	PL10D_3			
			PR10C_1	52	SPI_CS0
PMU_SUSCLK_CPLD	27	PB4C/CSSPIN_2	PR10D_1	51	XP1R8V_PGOOD
BIOS_DIS0_N	28	PB4D_2			
			PT9A_0	99	SPI_CS1
PMU_SLP_S3_N	29	PB6A_2	PT9B_0	98	VNNP_PGOOD
VCCP_EN	30	PB6B_2			
WDT_CON	31	PB6C/MCLK/CCLK_2	PT10A_0	97	XP1R24V_PGOOD
EMMC_RST_N	32	PB6D/SO/SPISO_2	PT10B_0	96	VCCP_PGOOD
			PT10C/TDO_0	95	CPLD_TDO
THRM_N	34	PB9A/PCLKT2_0_2	PT10D/TDI_0	94	CPLD_TDI
PWR_OK	35	PB9B/PCLKC2_0_2			
			PT11C/TCK_0	91	CPLD_TCK
XP1R05V_EN	38	PB11A/PCLKT2_1_2	PT11D/TMS_0	90	CPLD_TMS
SPI_CS_N	39	PB11B/PCLKC2_1_2			
EXCD1_PERST_N	36	PB11C_2	PT12A/PCLKT0_1_0	88	VCCP_PINALRT
SOC_ERR2_N	37	PB11D_2	PT12B/PCLKC0_1_0	87	VDDQP_PGOOD
			PT12C/SCL/PCLKT0_0_0	86	VDDQP_EN
VNNP_EN	40	PB15A_2	PT12D/SDA/PCLKC0_0_0	85	CPLD_MEMHOT_L
PMU_SLP_S45_N	41	PB15B_2			
			PT15A_0	84	VDDQP_PINALRT
XP1R05V_PGOOD	42	PB18A_2	PT15B_0	83	VCCRAMP_EN
I2C_SDA	43	PB18B_2	PT15C/JTAGENB_0	82	VCCRAMP_PGOOD
CB_RESET_N	45	PB18C_2	PT15D/PROGRAMN_0	81	THERMTRIP_N_CON
I2C_SCL	47	PB18D_2			
			PT16C_0	78	LPC_SERIRQ
XP0R6V_EN	48	PB20C/SN_2	PT17C/INITN_0	77	CPLD_MEMHOT_N
XP0R6V_PGOOD	49	PB20D/SI/SISPI_2	PT17D/DONE_0	76	CPLD_PROCHOT_N
			NC	89	

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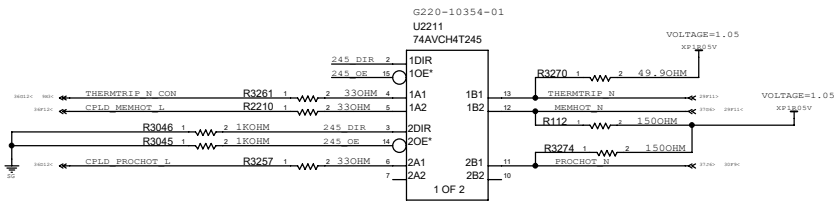


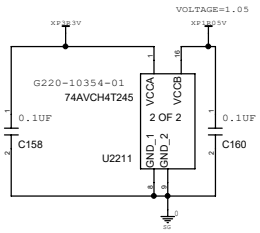


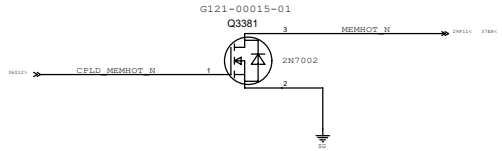
NOTE:
R130 ACTUALLY POP A 100PF CAP IN BOM TO FIX TCK ISSUE IN QUESTONE2
(CPLD ONLINE UPDATE FAILED ISSUE)

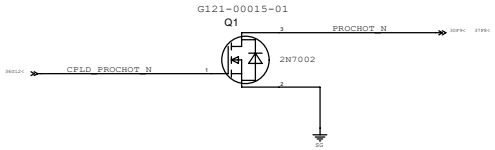
CPLD

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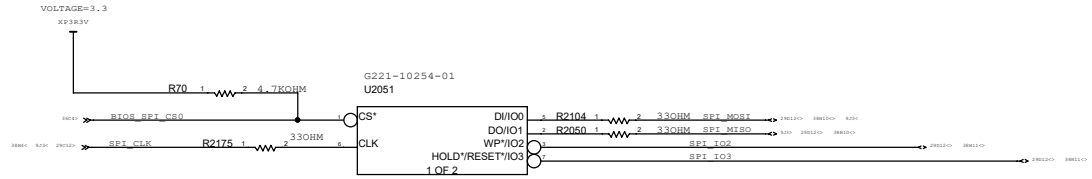


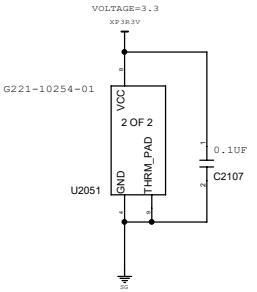


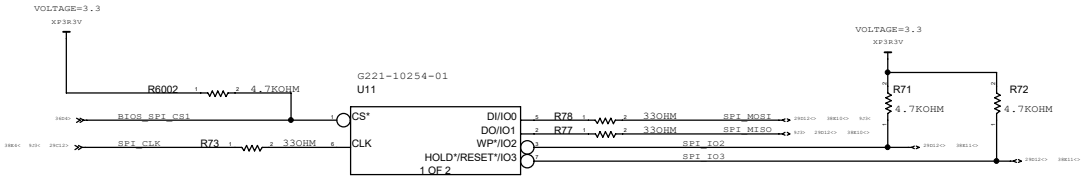
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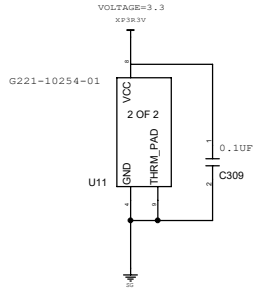
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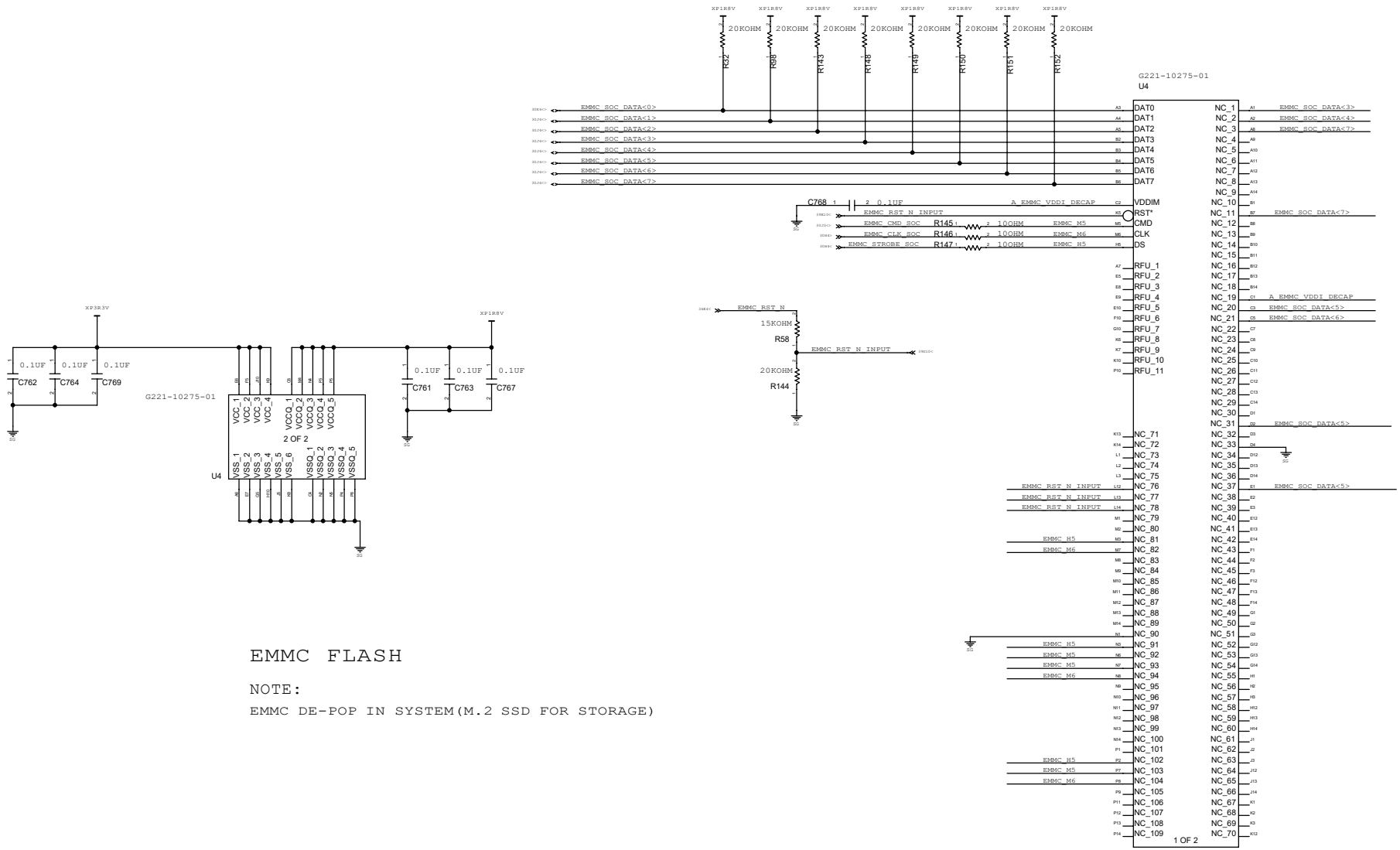


NOTE:
BIOS(U11,U2051) ALREADY POP IN COMM PRODUCT BASE BOARD
SO DE-POP IN BOM

BIOS

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EMMC FLASH

NOTE:

EMMC DE-POP IN SYSTEM(M.2 SSD FOR STORAGE)

EMMC FLASH

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CHANGE LIST

REV	CONTENT	REV	CONTENT
1.0	INITIAL REVIEW		
2.0	ADD CONN A48 PIN FOR SPI_TPM_CS_N USING		

CHANGE LIST

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